"SoC Technology Towards a New Era of Innovation"

ISOCC 2022

19th International SoC Design Conference

October 19-22, 2022

Lakai Sandpine Resort,
Gangneung-si, Gangwon-do, Korea

Organized by

ISE The Institute of Semiconductor Engineers · IEEE · CAS · IDEC IC DESIGN EDUCATION CENTER

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PROGRAM BOOK

"SoC Technology Towards a New Era of Innovation"

ISOCC 2022

19th International SoC Design Conference

October 19-22, 2022

Lakai Sandpine Resort, Gangneung-si, Gangwon-do, Korea

ISOCC 2022
19th International SoC Design Conference

CONTENTS

04_Foreword
05_Message from Technical Program Committee Chair
06_Invitation to ISOCC 2023
07_Committee
13_Time Table
16_Mini Tutorials
21_Main Tutorial
25_Short Tutorials
26_WiSoC Session
29_Opening Ceremony
30_Keynote Speeches
36_Technical Program
77_Chip Design Contest
85_Closing Ceremony
87_Special Program
91_Conference Information

FOREWORD

"Welcome to ISOCC 2022"

It is an honor to welcome you to the 19th International System-on-Chip Design Conference (ISOCC 2022) organized by the Institute of Semiconductor Engineers of Korea and financially co-sponsored by IEEE Circuits and Systems (CAS) Society. ISOCC is one of the most highly acclaimed annual conferences in the field of SoC. Since its inception, ISOCC has been continuing to showcase the most recent innovations and trends in the semiconductor system-on-a-chip area with active participation from worldwide researchers in academia, industry, and institutes. We are truly glad to host such a prestigious event at Gangneung-si, Gangwon-do, from October 19 through October 22 in 2022.

The conference theme is "SoC Technology Towards a New Era of Innovation". In this conference, we try to discuss key issues of advanced SoC technology for the new era of innovations and hurdles to realize the intelligent SoCs and to see what the future SoC will look like.

Researchers, engineers, and students, from industry, universities and government agencies will present their latest work and to discuss research and applications for system on chip designs. All participants will be sure to have a meaningful experience with industry peoples and scholars from around the world.

ISOCC 2022 hybrid conference will allow you to access an unparalleled amount of excellent content. You will be sure to have a meaningful experience with industry peoples and scholars from around the world. I hope you will enjoy not only the technical diversity of topics but also the natural beauty and culture of fantastic Gangneung, where ISOCC 2022 will be held, is a municipal city in the province of Gangwon-do, on the east coast of South Korea. Gangneung has many tourist attractions, such as Jeongdongjin, a very popular area for watching the sunrise, and Gyeongpo Beach. The city hosted all the ice events for the 2018 Winter Olympics. It takes two hours by KTX from Seoul to reach Gangneung.

I would like to extend my gratitude to all the contributors including organizing committee members, technical program committee members, steering committee members, reviewers, special session organizers, all the speakers invited, and authors. Also, I would like to thank all the sponsors for their support for the successful event.

We hope for the success of this conference and the safety of the participants.

Jongsun Park

Jongsun Park

General Chair, ISOCC 2022

MESSAGE FROM TPC CHAIR

On behalf of the Technical Program Committee, it is our pleasure to welcome you to the 19th International SoC Design Conference (ISOCC 2022) in Gangneung, Korea. ISOCC continues our tradition of showcasing the recent innovations and advancements in the System-on-Chip (SoC) area.

This year, the conference theme is "SoC Technology Towards a New Era of Innovation". The evolution of technology in the last decade has been multi-dimensional, and now we are at the center of a technology innovation. SoC technologies are playing a fundamental role for the innovation with various applications such as AIoT, 5G, bio-health and automotive semiconductor. ISOCC 2022 will share recent technology innovations that will accelerate future development in our society.

The ISOCC 2022 technical program consists of 199 outstanding papers over 30 technical sessions. Among them, 134 regular papers are presented at 16 oral sessions and 1 poster session, and 65 special session papers are presented at 13 special sessions. The 134 excellent papers are selected out of 188 regular submissions from 12 countries, which reflects the acceptance rate of 71.28 % and continuing internationalization of this conference.

The conference features 6 Keynote speeches by outstanding leading innovators of The Pennsylvania State University, Samsung Electronics, Skhynix, Synopsys, Siemens EDA, and Cadence to share their visions and prospects. It also features 8 educational tutorials and chip design contest demos (CDC) to promote the technical updates in SoC research and development.

I would like to express my sincere gratitude to all who have contributed to the technical program, including authors, reviewers, special session organizers, organizing committee members, and technical program committee members. ISOCC 2022 would not be possible without their devotions and efforts.

I wish that the technical program is enjoyable and satisfactory to all participants.

Seokhyeong Kang
Technical Program Committee Chair
ISOCC 2022

INVITATION TO ISOCC 2023

It is a great pleasure to invite you to the 20th International SoC Conference (ISOCC 2023), which will be held from October 23rd through October 26th in 2023 at RAMADA Hotel in Jeju island. This conference is one of the most highly acclaimed annual conferences in the field of SoC. We are truly glad to host such a prestigious event in the beautiful island, Jeju. Since its inception, ISOCC has been continuing to showcase the most recent innovations and trends in the semiconductor system-on-a-chip area with active participations from worldwide researchers in academia, industry, and institutes. The organizing and technical committee of ISOCC 2023 is gearing up for an exciting and advanced program including plenary speeches, invited talks, tutorials, technical paper presentations, and various social programs.

Jeju island has been the most favorite venue in ISOCC history for its beautiful volcanic island nature and convenient flight access from world. Jeju, as the southernmost and largest island of Korea, was created by volcanic eruptions that occurred millions of years ago. The island has significant academic values as well as marvelous natural landscapes. Dominated by Halla Mountain (1,950 m) at its center, Jeju also has many parasitic cones (called “Oreum”), vast open pastures, and lovely trekking courses (called ‘Olle-gil’). I believe that you will like Jeju if you are either the first-time visitor or have visited the island several times before.

All members of the ISOCC 2023 organizing committee look forward to seeing you and your valuable research works in Jeju, Korea, in ISOCC 2023.

We invite you to join us at the ISOCC 2023, where you will be sure to have a meaningful experience with industry peoples and scholars from around the world.

Sincerely,

Minjae Lee
General Chair
ISOCC 2023

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TIME TABLE

Regualr Session			
DCAS1	Memory Circuits	SoC1	Design Methodolyg
DCAS2	Memory Architecture and Systems	SoC2	Design Infrastructure
DCAS3	Digital Signal Processing	ET1	Emerging Technologies for Advanced Computing
DCAS4	Hardware Security Circuits	ET2	Emerging Technologies for Circuits and Systems
DCAS5	Communication Circuits and Systems	AC	Analog Circuits
ML1	Novel Algorithms for AI	DC	Advanced Data Converter
ML2	Circuits to Systems for AI	RF	Advanced Radio-Frequency Design Techniques
ML3	Near-Memory and Special Hardware for AI	WLN	Wireline

Special Session	
SS 1	Design and Testing Techniques for Computing-In-Memories
SS 2	Memory-Centric Accelerator Design for Deep Neural Network Applications
SS 3	Algorithm-or Architecture-Level Schemes for Reducing Operation Complexity of Neural Networks
SS 4	Design, Analysis and Tools for Integrated Circuits and Systems (DATICS)
SS 5	Emerging Applications and FPGA Implementation of Machine Learning
SS 6	Hardware Security, Reliability and Trust for SoCs
SS 7	Analysis and Design of Power and Energy Circuits and Systems
SS 8	Emerging Applications of Intelligent System Semiconductor
SS 9	Low Power Accelerator Design Utilizing Neural Networks for IoT Applications
SS 10	Emerging Techniques for Neural Networks, Non-linear, and Bio-related Circuits and Systems
SS 11	Circuits and Systems of Artificial Intelligence and Security
SS 12	Simulation and Analysis for Nonlinear Problems
SS 13	Design and Analysis of Nonlinear Circuits and Networks

<table>
<tr><th colspan="11">WEDNESDAY_ OCTOBER 19, 2022</th></tr>
<tr><th colspan="2"></th><th>Lobby</th><th>Lakai Ballroom 2</th><th>Lakai Ballroom 1</th><th>Sandpine</th><th>Cheon-Yeon</th><th colspan="2">Ho-Hae</th><th colspan="2">Hae-Woon</th></tr>
<tr><th>From</th><th>Till</th><th></th><th>Convention 1F</th><th>Convention 1F</th><th>Convention 1F</th><th>Reception B1F</th><th colspan="2">Tower 5 B1F</th><th colspan="2">Tower 5 B1F</th></tr>
<tr><td>13:00</td><td>13:15</td><td rowspan="20">On-site Registration</td><td rowspan="20"></td><td rowspan="20"></td><td rowspan="20"></td><td rowspan="9">Mini Tutorial</td><td rowspan="5">SS1</td><td>125</td><td rowspan="5">SS2</td><td>10</td></tr>
<tr><td>13:15</td><td>13:30</td><td>61</td><td>81</td></tr>
<tr><td>13:30</td><td>13:45</td><td>98</td><td>123</td></tr>
<tr><td>13:45</td><td>14:00</td><td>71</td><td>124</td></tr>
<tr><td>14:00</td><td>14:15</td><td></td><td>134</td></tr>
<tr><td>14:15</td><td>14:30</td><td colspan="4">Break Time (15min.)</td></tr>
<tr><td>14:30</td><td>14:45</td><td rowspan="5">SS3</td><td>67</td><td rowspan="5">SS4</td><td>96</td></tr>
<tr><td>14:45</td><td>15:00</td><td>86</td><td>119</td></tr>
<tr><td>15:00</td><td>15:15</td><td rowspan="5">Main Tutorial</td><td>115</td><td>126</td></tr>
<tr><td>15:15</td><td>15:30</td><td>187</td><td>131</td></tr>
<tr><td>15:30</td><td>15:45</td><td>209</td><td>132</td></tr>
<tr><td>15:45</td><td>16:00</td><td colspan="4">Break Time (15min.)</td></tr>
<tr><td>16:00</td><td>16:15</td><td rowspan="5">SS5</td><td>43</td><td rowspan="5">SS6</td><td>89</td></tr>
<tr><td>16:15</td><td>16:30</td><td>27</td><td>90</td></tr>
<tr><td>16:30</td><td>16:45</td><td>145</td><td>34</td></tr>
<tr><td>16:45</td><td>17:00</td><td>105</td><td>37</td></tr>
<tr><td>17:00</td><td>17:15</td><td>38</td><td>235</td></tr>
<tr><td>17:15</td><td>17:30</td><td>32</td><td>269</td></tr>
<tr><td>17:30</td><td>18:00</td><td colspan="10">Break Time (30min.)</td></tr>
<tr><td>18:00</td><td>20:00</td><td colspan="10">Welcome Reception</td></tr>
</table>

TIME TABLE

THURSDAY_ OCTOBER 20, 2022													
From	Till	Lobby	Lakai Ballroom 2 Convention 1F	Lakai Ballroom 1 Convention 1F	Sandpine Convention 1F		Cheon-Yeon Reception B1F		Ho-Hae Tower 5 B1F		Hae-Woon Tower 5 B1F	
08:15	08:30	On-site Registration	Chip Design Contest (CDC) Poster 1		CDC ORAL	CDC-O001						
08:30	08:45					CDC-O002						
08:45	09:00					CDC-O003						
09:00	09:15					CDC-O004						
09:15	09:30					CDC-O005						
09:30	09:45			Opening Ceremony (Lakai Ballroom1)								
09:45	10:35			Thursday_Keynote Speech-1 (Lakai Ballroom1)								
10:35	11:25			Thursday_Keynote Speech-2 (Lakai Ballroom1)								
11:25	11:35			Break Time (10min.)								
11:35	12:15			Thursday_Keynote Speech-3 (Lakai Ballroom1)								
12:15	12:30			WiSoC (with lunch)	Lunch (Hansong, Reception B1F)							
12:30	13:30											
13:30	13:45		Chip Design Contest (CDC) Poster 2		DCAS1	23	AC	218	SoC1	6	SS7	46
13:45	14:00					211		201		114		49
14:00	14:15					179		5		130		104
14:15	14:30					180		191		135		111
14:30	14:45					208				234		112
14:45	15:00			Break Time (15min.)								
15:00	15:15				DCAS2	215	DC	144	ET1	44	SS8	13
15:15	15:30					2		63		192		65
15:30	15:45					108		21		129		127
15:45	16:00					172		133		198		158
16:00	16:15					4		140		194		162
16:15	16:30		Chip Design Contest (CDC) Poster Exhibition									
16:30	16:45											
16:45	17:00				DCAS3	107	ML1	217	SS9	47	SS10	178
17:00	17:15					20		229		58		236
17:15	17:30					143		262		199		265
17:30	17:45					227		154		41		270
17:45	18:00					45		207				271
18:00	18:30	Break Time (30min.)										
18:30	20:30	Banquet (Skybay Hotel Gyeongpo, Grandball room(L floor))										

TIME TABLE

FRIDAY_ OCTOBER 21, 2022												
From	Till	Lobby	Lakai Ballroom 2 Convention 1F	Lakai Ballroom 1 Convention 1F	Sandpine Convention 1F		Cheon-Yeon Reception B1F		Ho-Hae Tower 5 B1F		Hae-Woon Tower 5 B1F	
08:30	08:45	On-site Registration			DCAS4	118	ML2	56	SS11	147	SS12	24
08:45	09:00					197		203		204		50
09:00	09:15					238		33		240		116
09:15	09:30					15		82		258		83
09:30	09:45					189		223		259		99
09:45	10:00			Break Time (15min.)								
10:00	10:50		Poster Exhibition Time	Friday_Keynote Speech-1 (Lakai Ballroom1)								
10:50	11:40			Friday_Keynote Speech-2 (Lakai Ballroom1)								
11:40	11:50			Break Time (10min.)								
11:50	12:30			Friday_Keynote Speech-3 (Lakai Ballroom1)								
12:30	12:40			Lunch (Hansong, Reception B1F)					Short Tutorial1		Short Tutorial2	
12:40	13:20											
13:20	14:00											
14:00	14:15				DCAS5	153	RF	232	SoC2	3	SS13	78
14:15	14:30					121		165		88		25
14:30	14:45					174		164		219		113
14:45	15:00					239		160		243		85
15:00	15:15					68		51				106
15:15	15:30			Poster Standing Time (30min.)								
15:30	15:45											
15:45	16:00				ML3	139	WLN	42	ET2	148		
16:00	16:15					181		29		177		
16:15	16:30					76		190		233		
16:30	16:45					195		55		150		
16:45	17:00					18		52		241		
17:00	17:15		Break Time (15min.)									
17:15	17:45		Closing Ceremony (Lakai Ballroom1)									

SATURDAY_ OCTOBER 22, 2022		
10:00	11:00	Committee Meeting & Discussion

Mini Tutorial 1

Chair | Woojoo Lee *(Chung-Ang University, Korea)*

13:00~13:20, WEDNESDAY_OCTOBER 19, 2022
Cheon-Yeon (Reception B1F)

Memory-based Hardware Neural System for High-density and Low-power Applications

Prof. Min-Hwi Kim
Assistant Professor, Chung-Ang University, Korea

Biography

Min-Hwi Kim received the B.S. and Ph.D degrees in electrical engineering from Seoul National University (SNU), in 2013 and 2020, respectively. From 2020 to 2022, He was a staff engineer with Samsung Electronics, Hwaseong-si, South Korea, where he has worked on the design of 3D NAND Flash memory. In 2022, he joined Chung-Ang University (CAU) as an Assistant Professor at the School of Electrical and Electronics Engineering (SoEEE). His research interests include the next generation semiconductor memory devices and energy-efficient neuromorphic electronics.

Abstract

Recently, the semiconductor industry and academia are facing limitations of existing computing system as the development of device scaling and process integration slows down. From this trend, new computing systems such as in-memory computing and neuro-inspired computing are emerging, and their applications to new fields are also expanding. In this presentation, we will first look into what is required for the implementation of memory-based high-density and low-power hardware neural system, and introduce the recent research achievements so far.

Mini Tutorial 2

Chair | Woojoo Lee *(Chung-Ang University, Korea)*

13:20~13:40, WEDNESDAY_OCTOBER 19, 2022
Cheon-Yeon (Reception B1F)

Multi-carrier modulation for ultra-high-speed ADC-based SerDes

Prof. Gain Kim
Assistant Professor,
Daegu Gyeongbuk Institute of Science & Technology (DGIST), Korea

Biography

Gain Kim received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from the Ecole Polytechnique Federal de Lausanne (EPFL), Lausanne, Switzerland in 2013, 2015, and 2018 respectively. From 2016 to 2018, he was with IBM Research Zurich, working on ADC-based wireline receiver designs. From 2018 to 2020, he was with KAIST as a postdoctoral fellow, and from Nov. 2020 to Jan. 2022 he was with Samsung Research, Seoul, South Korea, as a staff engineer working on a baseband modem for 6G wireless communications. In Jan. 2022, he joined Daegu Gyeongbuk Institute of Science & Technology (DGIST), Daegu, South Korea, where he is currently an assistant professor. His current research interests include the design of high-speed ADC, ultra-high-speed SerDes design, modulation techniques for ADC-based serial links, as well as multi-chip computing systems with energy-efficient interfaces.

Abstract

With the increasing data rate to 112Gb/s per lane, PAM-4 with ADC-based RX has become the most commonly employed modulation for ultra-high-speed serial links. To keep the data-rate increasing beyond 200Gb/s/lane, modulation techniques exhibiting high bandwidth efficiency have been investigated for multiple reasons, such as reduced attenuation and lower required DAC/ADC conversion rate. With a particular emphasis on orthogonal frequency division multiplexing (OFDM), this talk covers link modeling with OFDM, design-space exploration, and implementation challenges for enabling a data rate of 200Gb/s and beyond in wireline transceivers.

Mini Tutorial 3

Chair | Woojoo Lee *(Chung-Ang University, Korea)*

13:40~14:00, WEDNESDAY_OCTOBER 19, 2022
Cheon-Yeon (Reception B1F)

Trends of Modern Processors for AI Acceleration

Prof. Kyuho Lee
Assistant Professor,
Ulsan National Institute of Science & Technology (UNIST), Korea

Biography

Kyuho Lee received B.S., M.S., and Ph. D. degrees in the School of Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea in 2012, 2014, and 2017, respectively. Now he is an Associate Professor at the Department of Electrical Engineering and the Graduate School of Artificial Intelligence, Ulsan National Institute of Science and Technology (UNIST). He is serving as a TPC member of IEEE Asian Solid-State Circuits Conference and ACM/IEEE Design, Automation and Test in Europe since 2018. Before joining UNIST as a faculty member, he had worked for Samsung Research America, Richardson, TX, USA as a hardware designer in 2016. From 2017 to 2018, he was a postdoctoral researcher in the Information Engineering and Electronics Research Institute, KAIST, Daejeon, Korea. His research interests include mixed-mode neuromorphic SoC, deep learning processor, Network-on-Chip architectures, and intelligent computer vision processor for mobile devices and autonomous vehicles.

Abstract

Machine learning and artificial intelligence technology are playing the key role in the 4th industrial revolution and tremendous amount of researches are actively conducted to blend the technologies into our daily lives with practical applications such as autonomous vehicles/robots/drones, AI speaker, smart surveillance, etc. Most of current works rely on GPU that is not a practical solution to embedded systems and mobile platforms due to its large form factor and power consumption. Instead, low-power hardware accelerators are essential for feasible implementation and they have been investigated recently with different aspects and architectures. In this talk, I will review the technological challenges and trends in latest AI accelerators as well as introducing practical systems on AI applications.

Mini Tutorial 4

Chair | Woojoo Lee *(Chung-Ang University, Korea)*

14:00~14:20, WEDNESDAY_OCTOBER 19, 2022
Cheon-Yeon (Reception B1F)

A miniaturized wireless neural implant with body-coupled power delivery and data transmission

Prof. Joonsung Bae
Assistant Professor, Kangwon National University, Korea

Biography

Joonsung Bae graduated from the Electrical Engineering Department of Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2007 and received the M.S. and Ph.D. degrees in electrical engineering from the KAIST in 2009 and 2013, respectively. His Ph.D. work concerned the Wireless Body Area Network (WBAN) circuits and systems.
Since 2017, he has been with the Department of Electrical and Electronics Engineering, Kangwon National University, where he is currently an Associate Professor. Before joining Kangwon National University, he was an Analog Circuit Designer with IMEC, Belgium, where he investigated ultra-low-power biomedical circuits. His current research interests are energy-efficient mixed-signal circuits and systems, wireless neural interfaces, bio-medical integrated sensors, and body area networks.

Abstract

This talk presents the design, implementation, and validation of a wireless neural implant that uses body-coupled power delivery and data transmission, considering closed-loop multichannel wireless neural interfaces. The scheme is applicable to a central nervous system based on: 1) its use of bidirectional communications combined with wireless reception without recourse to customized and dedicated antennas or transducers and 2) its exploitation of an undemanding electrode interface and the conductive properties of the body. From the details of body-coupled channel characteristics, the implementation of the power receiver and data transceivers to the prototyped system using integrated circuits are introduced, demonstrating its feasibility in miniaturized wireless neural implant applications.

Mini Tutorial 5

Chair | Woojoo Lee *(Chung-Ang University, Korea)*

14:20~14:40, WEDNESDAY_OCTOBER 19, 2022
Cheon-Yeon (Reception B1F)

Augmented Reality 3D Head-up Display Systems

Prof. Dongwoo Kang
Assistant Professor, Hongik University, Korea

Biography

Dongwoo Kang received the B.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2007, and the M.S. and Ph.D. degrees in electrical engineering from University of Southern California, Los Angeles, CA, in 2009 and 2013, respectively. He was a Senior Researcher at at Samsung Advanced Institute of Technology, Suwon, South Korea, from 2013 to 2021. In 2021, he joined the faculty of the department of electronic and electrical engineering at Hongik University, Seoul, South Korea, where he is currently an Assistant Professor. His research interests include image processing and computer vision algorithm including detection, tracking, segmentation, image enhancement for augmented reality 3D displays and medical images.

Abstract

Eye pupil tracking is important for augmented reality (AR) three-dimensional (3D) head-up displays (HUDs). Accurate and fast eye tracking is still challenging due to multiple driving conditions with eye occlusions, such as wearing sunglasses. We presents a AR 3D HUD system for commercial use that can handle practical driving conditions. Our system classifies human faces into bare faces and sunglasses faces, which are treated differently. Experiments show that our method achieves high accuracy and speed, approximately 1.5 and 6.5 mm error for bare and sunglasses faces, respectively, at less than 10 ms on a 2.0GHz CPU. The proposed method, combined with AR 3D HUDs, shows promising results for commercialization with low crosstalk 3D images.

ISOCC 2022
19th International SoC Design Conference

Main Tutorial
WEDNESDAY, OCTOBER 19

Main Tutorial

Chair | Jungrae Kim *(Sungkyunkwan University, Korea)*

15:00~16:30, WEDNESDAY_OCTOBER 19, 2022
Cheon-Yeon (Reception B1F)

Fault and Soft-Error Tolerant DLL Design for Heterogeneous Multi-Die Clock Synchronization

Prof. Shi-Yu Huang
Electrical Engineering,
National Tsing Hua University, Taiwan

Biography

Shi-Yu Huang received his B.S. and M.S. degrees from Electrical Engineering Dept., National Taiwan University, from 1988 and 1992, respectively, and his Ph.D. degree in Electrical and Computer Engineering from University of California, Santa Barbara, in 1997. Since 1999, he has joined National Tsing Hua University, Taiwan until now. His recent research is concentrated on all-digital timing circuit designs, such as all-digital phase-locked loop (PLL), all-digital delaylocked loop (DLL), time-to-digital converter (TDC), and their applications to parametric fault testing and reliability enhancement for 3D-ICs. He has published more than 160 technical papers (including 46 IEEE journal papers). Dr. Huang ever co-founded a company in 2007-2012, TinnoTek Inc., specializing a cell-based PLL compiler and system-level power estimation tools. He is a co-author receiving the best presentation award or best-paper award for 5 times, (e.g., VLSI-DAT'2006, VLSI-DAT'2013, ATS'2014, WRTLT'2017, ISOCC'2018).

Prof. Huang is a senior member of IEEE. He has been a tutorial speaker in a number of prior IEEE conferences, (e.g., ATS'20, ITC-Asia'20, ITC-India'20, ISOCC'21, ITC'21, ATS'21). The topics include "Testing Clock and Power Networks", "Testing and Monitoring of Die-to-Die Interconnects

in a 2.5D/3D IC", and "Designing a DLL Easily Using Only Standard Cells for Clock Synchronization in A Heterogeneous Multi-Die IC".

Abstract

When we design an SoC or a multi-die IC consisting of 3rd-party IPs, heterogeneous components, or functional dice, synchronization of the clock signals across all of them could be a headache. Fortunately, Delay-Locked Loop (DLL) comes to the rescue. However, a DLL is traditionally built with some analog circuitry inside and thus making the design process complicated if not mysterious for system integrators. The emergence of cell-based DLL design style over the past two decades has alleviated this problem greatly. A cell-based DLL design is not only small, but also robust to the process and temperature variation. Also, it could lend itself to automation as a DLL compiler and so one can generate a DLL instance on the push of a button.

In this tutorial, we will take on a step-by-step journey to show you how to make your own robust and testable fault-tolerant DLL using only standard cells. In the first part, specific topics for the design of a basic DLL such as phase detector, tunable delay line, phase-locking procedure will be briefly reviewed. In the second part, Fault and soft-Error Tolerant (FET) DLL architecture, featuring static timing correction and dynamic timing correction schemes to keep the phase error small while withstanding the attack of run-time faults or soft errors. Finally in the third part, we will touch upon the online DLL monitoring schemes which are often necessary to make a FET DLL truly trustworthy throughout its entire lifecycle.

ISOCC 2022
19th International SoC Design Conference

Short Tutorials
FRIDAY, OCTOBER 21

Sensor with U Session

Short Tutorial 1

Chair | Jungrae Kim *(Sungkyunkwan University, Korea)*

12:40~13:20, FRIDAY_OCTOBER 21, 2022
Ho-Hae (Tower 5 B1F)

The Turn of Moore's Law from Space to Time – The Crisis, The Perspective and The Strategy

Liming Xiu
Chief Scientist of IC Technology and VP of Research,
BOE Technology Group, China

Biography

Liming Xiu earned B.S. and M.S. degrees in physics from Tsinghua University, China, in 1986 and 1988, respectively. He earned an MEEE degree from Texas A&M University, USA, in 1995. From 1995 to 2009, he worked for Texas Instruments, Dallas, USA, as a senior member of the Technical Staff. From 2009 to 2012, he was the chief clock architect of Novatek Microelectronics, Taiwan. From 2012 to 2015, he was VP for research at Kairos Microsystems, Dallas, USA. Since 2015, he has worked for BOE Technology Group, Beijing, China, as chief scientist of IC technology and VP for research. He served as VP of IEEE CASS from 2009 to 2010. He is the inventor of the Flying-Adder frequency synthesis architecture and an advocate of the time-average-frequency concept and theory. He has 36 US patents. He has published numerous IEEE journal and conference papers, four books as the sole author, and three book chapters as an invited author.

Abstract

A space-induced crisis is recognized as the cause of trouble that Moore's Law is currently facing. The contemporary practice of this empirical law is considered as happening within a space-dominant paradigm. An alternative of exploiting potential in the dimension of time is identified as an emerging paradigm in microelectronics. The new practice is termed a time-oriented paradigm. It is justified as the turn of Moore's Law from space to time. The resultant Time-Moore strategy is envisioned as the next-generation enabler for continuing Moore's Law's pursuit of everhigher information processing power and efficiency. It also serves as the perpetuation of the spirit that Moore's law is nothing but a collective storied history of innovations. In the first part of this tutorial, by following Thomas Kuhn's seminal work around the concepts of paradigm and scientific revolution, the argument for the Time-Moore strategy (Time-Moore: to use time more) and the paradigm shift from space to time is carried out through philosophical persuasion rather than technical proof due to the difficult challenge of change-of-mindset. The second part provides solid technical materials for supporting this transition from the old paradigm to the new one. The goal of this tutorial is to reevaluate the contemporary practice of microelectronics, identify the cause of the current crisis, advocate a change-of-mindset to circumvent the crisis, and ultimately point out a new route for advancing. After achieving so many unprecedented accomplishments through several decades of relentless endeavor, it's time for the big ship of Moore's Law to make a turn.

Siliconmitus Session

Short Tutorial 2

Chair | Suk-Ju Kang *(Sogang University, Korea)*

12:40~13:20, FRIDAY_OCTOBER 21, 2022
Hae-Woon (Tower 5 B1F)

Designing Efficient Deep Neural Network Training Processor

Prof. Dongsuk Jeon
Associate Professor, Seoul National University, Korea

Biography

2009, B.S. in electrical engineering, Seoul National University
2014, Ph.D. in electrical engineering, University of Michigan, Ann Arbor
2014 – 2015, Postdoctoral Associate, MIT
2016 – Present, Assistant/Associate Professor, Seoul National University

Abstract

Deep learning algorithms gathered serious attention due to their outstanding performance in various tasks. Their application areas are fast expanding from computer vision and speech recognition to multi-modal understanding. While power-saving techniques such as quantization, network compression, and pruning have been successfully adopted in pre-trained models, they often become next to useless when applied to the training process. This talk will discuss various algorithmic and hardware optimization techniques enabling energy-efficient training processors.

SAPEON Korea Inc Session

WiSoC 1

Chair | Hayun Chung *(Korea University, Korea)*

12:30~13:30, THURSDAY_OCTOBER 20, 2022
Lakai Ballroom 1 (Convention 1F)

Integrated Circuit and System Technologies for Neural Interface Devices

Prof. Yaoyao Jia
Assistant Professor, Electrical and Computer Engineering,
The University of Texas at Austin, USA

Biography

Dr. Yaoyao Jia received her Ph.D. degree from Georgia Tech in 2019. Currently, she is an assistant professor in the electrical and computer engineering department at the University of Texas at Austin and a Fellow of Silicon Labs Chair in electrical engineering. Her research primarily focuses on analog and mixed-signal integrated circuits, inductive, ultrasonic, and thermoelectric energy harvesting, the Internet of Medical Things (IoMT), implantable biomedical devices, miniature neural Interface implants, and wearable devices. Dr. Jia received the 2022 Micromachines Best Paper Awards, the 2019 IEEE Biomedical Circuits and Systems Conference (BioCAS) best paper award, the IEEE Solid-State Circuits Society (SSCS) predoctoral achievement award, and the 2015 IEEE BioCAS best live demo award. She is serving as the Associate Editor of IEEE Transactions on Biomedical Circuits and Systems (TBioCAS). She is also serving on the Technical Program Committee of IEEE Biomedical Circuits and Systems Conference (BioCAS) and IEEE Custom Integrated Circuits Conference (CICC).

Abstract

Neural interface devices that establish a direct communication pathway with the nervous system not only help deepen our understanding of the brain but also enable neuromodulation-based therapies for neurological disorders, e.g., Parkinson's disease, Alzheimer's disease, etc. My team aims to explore novel circuit topologies and system architectures to develop state-of-the-art neural interface devices. First, the major trends in the development of neural interface devices will be introduced. Next, our recent work on the development of neural interface devices, spanning from low-power ASIC designs to wireless power and data transmission strategies, will be presented. Finally, future expectations on how to address the remaining challenges in bioelectronics will be discussed to conclude this presentation.

WiSoC 2

Chair | Hayun Chung *(Korea University, Korea)*

12:30~13:30, THURSDAY_OCTOBER 20, 2022
Lakai Ballroom 1 (Convention 1F)

Seamless Solution for Immersive Transformation

Prof. Chae Eun Rhee
Professor, Information and Communication Engineering,
Inha University, Korea

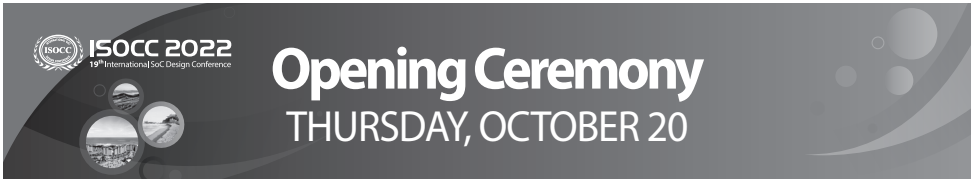
Biography

Chae Eun Rhee received the B.S., M.S. and Ph.D. degrees in Electrical Engineering and Computer Science from Seoul National University, Seoul, Korea, in 2000, 2002, and 2011, respectively. From 2002 to 2005, she was with the Digital TV Development Group, Samsung Electronics Company Ltd., Suwon City, Korea, as an Engineer, where she was involved in bus architecture and MPEG decoder development. In 2013, she joined the Department of Information and Communication Engineering at Inha University, Korea. Her research interests include algorithm/architecture design of immersive video for the AR/VR/MR systems, deep-learning hardware accelerator, and processing-in-memory.

Abstract

Many industries are preparing for digital transformation for the post-corona era. People demand more personalized video content, and at the same time, they pursuit a metaverse to communication and experience together. This talk introduces a study on the establishment of a plug-and-play-based immersive media integration platform that enables system-level performance verification for research in the rapidly developing immersive media field. Our platform aims to organically connect all processes of acquisition, processing, appreciation, and sharing for immersive media, and to enable seamless transformation from current 2-dimenstional image data to immersive media environments.

OPENING CEREMONY



09:30~09:45 THURSDAY, OCTOBER 20, 2022
Lakai Ballroom 1 (Convention 1F)

Welcome Address

Jongsun Park, General Chair *(Korea University, Korea)*

Conference Statistics

Seokhyeong Kang, Technical Program Committee Chair
(Pohang University of Science and Technology(POSTECH), Korea)

Announcements

Seokhyeong Kang. Technical Program Committee Chair
(Pohang University of Science and Technology(POSTECH), Korea)

Keynote Speech 1

09:45~10:35, THURSDAY_OCTOBER 20, 2022
Lakai Ballroom 1 (Convention 1F)

Ferroelectric-based Logic and Memory Architectures

Prof. Vijaykrishnan Narayanan
Professor, Electrical Engineering and Computer Science,
The Pennsylvania State University, USA

Biography

Vijaykrishnan Narayanan is the Robert Noll Chair of Computer Science and Engineering at The Pennsylvania State University. His research interests are in computer architecture, design using emerging technologies, and embedded systems. He is a recipient of the 2021 IEEE Computer Society Edward McCluskey Technical Achievement Award, and 2021 IEEECS TCVLSI Distinguished Research Award. He serves as the Associate Director of the DoE 3DFeM Center and a thrust leader for the DARPA/SRC Center for Brain Inspired Computing. He is a Fellow of the IEEE, ACM and National Academy of Inventors.

Abstract

In the last decade, there have been major changes in the families of ferroelectric materials available for integration with CMOS electronics. This talk will discuss the possibility of exploiting the 3rd dimension in microelectronics for functions beyond interconnect optimization, enabling 3D non-von Neumann computer architectures exploiting ferroelectrics for local memory, logic in memory, digital/analog computation, and neuromorphic/reconfigurable functionality. This approach circumvents the end of Moore's law in 2D scaling, while simultaneously overcoming the "von Neumann bottleneck" in moving instructions and data between separate logic and memory circuits. The talk will cover circuit and architectural features leveraging the non-volatile properties of ferro-electric FETs for hardware obfuscation, accelerator designs and in-memory compute structures.

Samsung Electronics Session

Keynote Speech 2

10:35~11:25, THURSDAY_OCTOBER 20, 2022
Lakai Ballroom 1 (Convention 1F)

Emerging trends and opportunities in Automotive Semiconductors

Dr. Haechang Lee
Executive Vice President, Automotive Sensor Team, System LSI Business,
Samsung Electronics, Korea

Biography

Haechang Lee is currently EVP of Engineering at Samsung Electronics where he oversees the automotive sensor development and business. He received the B.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA. He is an expert in semiconductor design and his experience spans sensors, MEMS, high speed data communications, and precision mixed signal systems. Prior to Samsung, he held leadership positions at Google, Altera, and SiTime.

Abstract

Four major trends – electrification, autonomous driving, connectivity, and centralized compute – are transforming automobile design and the semiconductors that enable them. As a result the automotive semiconductor market is expected to grow by more than 10% annually from $56 billion in 2022 to more than $140 billion in 2030. We will survey the industry and highlight the areas ripe for strong growth resulting from these trends. The second part of the talk will focus in on automotive sensors, critical to autonomous driving, and the technologies that are critical to this application.

Synopsys Session

Keynote Speech 3

11:35~12:15, THURSDAY_OCTOBER 20, 2022
Lakai Ballroom 1 (Convention 1F)

The Rise of Artificial Intelligence for Chip Design – Journey Thus Far and the Road Ahead

Dr. Joe Walston
Distinguished Architect, Distinguished Architect, Synopsys, USA

Biography

Dr. Joe Walston is a distinguished architect and a founding member of the machine learning center of excellence program at Synopsys. He has been designing AI solutions at Synopsys for more than 5 years and is the chief architect of DSO.ai, world's 1st AI application for chip design. Prior to this work, he led implementation methodology development for high-performance designs for nearly 20 years; first for Magma, then Synopsys. By using traditional techniques and developing novel ML solutions, Joe has enabled designers achieve highest PPA on processor IP in performance-critical, schedule-limited SoC projects. Joe holds a doctorate in Physics from North Carolina State University, and has authored 7 patents on AI and ML technology application.

Abstract

AI-designed chips are a reality. Samsung confirmed this a year ago with world's first use of AI to design a mobile processor chip. Since then, AI for design has been adopted across the industry at a phenomenal pace, accelerating silicon innovations to market in automotive, high-performance computing, consumer electronics, and other applications. Will this pace of innovation continue and ultimately lead to self-designed silicon? In this session, we will be looking at real-world examples as we travel through the past, present and future for AI in chip design.

Keynote Speech 1

10:00~10:50, FRIDAY_OCTOBER 21, 2022
Lakai Ballroom 1 (Convention 1F)

Machine Learning Empowered Functional Verification: Status, Challenges and Future

Dan Yu
Solution Manager AI/ML, Design Verification Technology,
Siemens EDA, USA

Biography

Dan Yu is Solution Manager of Design Verification at Siemens EDA. Prior to this work, Dan worked in Siemens Digital Industry and Corporate Technology in Germany, China and US. He had extensive experience on the AI/ML research and applications in various industrial domains. His works have been empowering many successful industrial products. He is a laureated inventor of the year in Siemens, with more than 70 patents on industrial AI and IoT applications. Dan holds a Master degree from Munich University and Technology.

Abstract

With the complexity of IC grows exponentially, any failure becomes more and more expensive to fix down the IC realization pipeline. FV Functional verification (FV) as the first step to ensure the quality of IC design, is becoming a bottleneck of productivity. FV is computation- and data-intensive by its nature, which makes it a perfect playground of machine learning (ML) applications. In this presentation we will give comprehensive overview and up-to-date survey of FV problems that are being and can be addressed by ML. Among the various ML techniques, several emerging ones e.g. transformers and graph neural networks are especially powerful in solving many FV problems. The presentation will then shed light on critical challenges for ML to be widely adopted and applied in production environment for FV and EDA in general, discuss how we should get ready for the next generation FV empowered by ML.

Keynote Speech 2

10:50~11:40, FRIDAY_OCTOBER 21, 2022
Lakai Ballroom 1 (Convention 1F)

Memory based Accelerator solution in AI era

Dr. Eui-cheol Lim
Fellow, Memory Solution Product Design Team, SK Hynix, Korea

Biography

Eui-cheol Lim is a Research Fellow and leader of Memory Solution Product Design team in SK Hynix. He received the B.S. degree and the M.S. degree from Yonsei University, Seoul, Korea, in 1993 and 1995, and the Ph.D. degree from Sungkyunkwan University, suwon, Korea in 2006. Dr.Lim joined SK Hynix in 2016 as a system architect in memory system R&D. Before joining SK Hynix, he had been working as an SoC architect in Samsung Electronics and leading the architecture of most Exynos mobile SoC. His recent interesting points are memory and storage system architecture with new media memory and new memory solution such as CXL memory and Processing in Memory.

Abstract

Various services using AI are becoming mainstream, and as the AI model size increases, the service range is also expanding. Accordingly, it requires more computing performance and more memory capacity. Technically, as you can see in the Go match between AlphaGo and Lee Sedol, the energy efficiency of AI computer system is fairly poor comparing with that of human brain. As a countermeasure against it, in this talk, Processing in Memory will be presented as one of the solutions. PIM architecture basically enables higher performance and lower energy consumption when performing memory intensive workloads. The current trending transformer based generative deep learning model, such as GPT2/3 shows memory intensive characteristics. The data analytics pipeline that pre-process and supplies data to the AI model also has a memory intensive feature. So, It is expected that PIM technology can be applied to the overall AI service computing system. In this talk, we'd like to introduce not only SK hynix's 1st PIM product, GDDR6-AiM, but also CXL memory card based PIM solution and storage level PIM solution. And finally, the concept of `data hierarchy' that applies PIM to all memory layers will be introduced as well.

Cadence Session

Keynote Speech 3

11:50~12:30, FRIDAY_OCTOBER 22, 2022
Lakai Ballroom 1 (Convention 1F)

Leveraging AI and Data Analytics to Make Faster Chips in Less Time

Dr. Venkat Thanvantri
Vice President, Research and Development,
Digital and Signoff Group – AI/ML, Cadence Design Systems, USA

Biography

Dr Venkat Thanvantri is VP of R&D at Cadence where he leads the AI/ML development for the Digital and Signoff Products. Venkat holds a Ph.D. from the University of Florida and a Master's from the Indian Institute of Science, Bangalore. He has over 20 years of experience in developing, managing, and deploying multiple EDA tools in the areas of timing, extraction, characterization, power, and place & route.

Abstract

As the semiconductor industry enters a new era of technological innovations and advancements, companies are looking for ways to improve performance and accelerate productivity. With generational technology drivers like, 5G, AI and autonomous driving and shortened time to market demands, traditional disciplines and methodologies of chip design require a fundamental transformation. In this presentation we will review how customers are applying Machine Learning based engines to automate the design flow and deploying state-of-the-art cloud enabled Data Analytics platforms to address these demands and looking at the future of AI in EDA.

Cadence Session

DCAS1 Memory Circuits

Chair | Yeongkyo Seo *(Inha University, Korea)*

13:30~14:45, THURSDAY_OCTOBER 20, 2022
Sandpine (Convention 1F)

DCAS1-1 (23) 13:30-13:45
Temperature Compensation on SRAM-Based Computation in Memory Array
Qibang Zang[1,2], Wang Ling Goh[1], Fei Li[2], Lu Lu[2], and Anh Tuan Do[2]
[1]Nanyang Technological University, Singapore
*[2]A*STAR, Singapore*

DCAS1-2 (211) 13:45-14:00
Source-Line Shared SOT-MRAM Cell for Energy Efficient Read Operation
Taehwan Kim and Jongsun Park
Korea University, Korea

DCAS1-3 (179) 14:00-14:15
SRAM Bit-line Boosting Circuit for Low Latency and Timing Aware Read Operation
Hyeyeong Lee, Joonhyung Kim, and Jongsun Park
Korea University, Korea

DCAS1-4 (180) 14:15-14:30
Bit-Line Decoupled SRAM for Reducing Read Delays in Near Threshold Voltage Operations
Hyunchul Park and Jongsun Park
Korea University, Korea

DCAS1-5 (208) 14:30-14:45
Energy-Efficient STT-MRAM based Digital PIM supporting Vertical Computations Using Sense Amplifier
Yeseul Kim and Jongsun Park
Korea University, Korea

ORAL SESSIONS

KETI Session

AC Analog Circuits

Chair | Min-Seong Choo *(Hanyang University, Korea)*

13:30~14:45, THURSDAY_OCTOBER 20, 2022
Cheon-Yeon (Reception B1F)

AC-1 (218)
13:30-13:45

Fast-Transient LDO Regulator with RC-less Low- Impedance Buffer and PVT Compensation

Tzung-Je Lee and Hung-Hsiang Chang

National Sun Yat-Sen University, Taiwan

AC-2 (201)
13:45-14:00

A Design of high-efficiency Constant On-Time Control DC-DC Buck Converter for Power Management integrated circuits

Qurat ul Ain, Muhammad Basim, Syed Adil Ali Shah, and Kang-Yoon Lee

Sungkyunkwan University, Korea

AC-4 (5)
14:00-14:15

A Fully Differential Switched Capacitor Amplifier with a Two-Stage Folded-Mesh Class AB Operational Amplifier in a 22 nm FD-SOI CMOS Process

Jeongwook Koh[1] and Elmar Herzer[2]

[1]Fraunhofer Institute for Integrated Circuits IIS, Division Engineering of Adaptive Systems EAS, Dresden, Germany
[2]Fraunhofer Institute for Integrated Circuits IIS, Erlangen, Germany

AC-5 (191)
14:15-14:30

Wide Dynamic Range Temperature Sensor Using High Sensitivity PTAT Current Generator

Tzung-Je Lee and Kuo-Hsun Tu

National Sun Yat-Sen University, Taiwan

TechwidU Session

SoC1 Design Methodolyg

Chair | Daijoon Hyun *(Cheongju University, Korea)*

13:30~14:45, THURSDAY_OCTOBER 20, 2022
Ho-Hae (Tower 5 B1F)

SoC1-1 (6) 13:30-13:45
A Layout Generator of Latch, Flip-Flop, and Shift Register for High-Speed Links
Junung Choi, Jaeik Cho, Won Joon Choi, Myungguk Lee, and Byungsub Kim
Pohang University of Science and Technology (POSTECH), Korea

SoC1-2 (114) 13:45-14:00
An Improved Early Termination Methodology Using Convolutional Neural Network
Seung Ho Shin , Hayoung Lee, Sooryeong Lee, Younwoo Yoo, and Sungho Kang
Yonsei University, Korea

SoC1-3 (130) 14:00-14:15
PROG: Per-Row Output Generator for BOST
Sooryeong Lee, Hayoung Lee, Younwoo Yoo, Seung Ho Shin, and Sungho Kang
Yonsei University, Korea

SoC1-4 (135) 14:15-14:30
Pair-Grouping Scan Chain Architecture for Multiple Scan Cell Fault Diagnosis
Sunghoon Kim, Seokjun Jang, Youngki Moon, and Sungho Kang
Yonsei University, Korea

SoC1-5 (234) 14:30-14:45
FACTGen: Framework for Automated Circuit Topology Generator
Jangwon Suh and Wanyeong Jung
Korea Advanced Institute of Science and Technology(KAIST), Korea

ORAL SESSIONS

DB HiTek Session

DCAS2 Memory Architecture and Systems

Chair | Youngjoo Lee *(Pohang University of Science and Technology(POSTECH), Korea)*

15:00~16:15, THURSDAY_OCTOBER 20, 2022
Sandpine (Convention 1F)

DCAS2-1 (215) 15:00-15:15
Distributed Accumulation based Energy Efficient STT-MRAM based Digital PIM Architecture
Dongsu Kim and Jongsun Park
Korea University, Korea

DCAS2-2 (2) 15:15-15:30
FAME: Fault Address Memory Structure for Repair Time Reduction
Hayoung Lee, Sooryeong Lee, Younwoo Yoo, Seung Ho Shin, and Sungho Kang
Yonsei University, Korea

DCAS2-3 (108) 15:30-15:45
Hiding Precharge Operation For Improved SRAM Cycle Time
Yoojeong Yang, Dain Chon, and Woong Choi
Sookmyung Women's University, Korea

DCAS2-4 (172) 15:45-16:00
High Detection Rate BCH Code with CRC Code for Memory Application
Minseo Kim and Jongsun Park
Korea University, Korea

DCAS2-5 (4) 16:00-16:15
YOCO: Unified and Efficient Memory Protection for High Bandwidth Memory
Dongwhee Kim and Jungrae Kim
Sungkyunkwan University, Korea

MetaCNI Session

DC | Advanced Data Converter

Chair | Minseob Shim *(Gyeongsang National University, Korea)*

15:00~16:15, THURSDAY_OCTOBER 20, 2022
Cheon-Yeon (Reception B1F)

DC-1 (144) 15:00-15:15
Second-order Incremental Delta-sigma Modulator with 3-bit SAR ADC and Capacitor Sharing Scheme
Wonkyu Do, Neungin Jeon, Hoyong Jung, and Young-Chan Jang
Kumoh National Institute of Technology, Korea

DC-2 (63) 15:15-15:30
A 10.12μW 101.98dB-SNDR Three-step Incremental Analog-to-Digital Converter
Huaikun Ji, Zhenhao Fan, Zhaonan Lu, Zhichao Tan, and Menglian Zhao
Zhejiang University, China

DC-3 (21) 15:30-15:45
An Improved Dynamic Latch Comparator with Low Power Consumption for SAR ADC Applications
Phanidarapu Mounika, Deeksha Verma, and Kang-Yoon Lee
Sungkyunkwan University, Korea

DC-4 (133) 15:45-16:00
Just-Enough Strategy for Accurate Clock Jitter Measurement Using A Cyclic Time-to-Digital Converter
Yung-Chuan Su and Shi-Yu Huang
National Tsing Hua University, Taiwan

DC-5 (140) 16:00-16:15
A 8-bit 300MHz Domino Based Successive Approximation Register ADC
Ko-Chi Kuo[1] and Hsiung-Yu Chi[2]
[1]National Sun Yat-sen University, Taiwan
[2]Sunplus Technology Co., Ltd, Taiwan

ORAL SESSIONS

Telechips Session

ET1 Emerging Technologies for Advanced Computing

Chair | Hyung-Min Lee *(Korea University, Korea)*

15:00~16:15, THURSDAY_OCTOBER 20, 2022
Ho-Hae (Tower 5 B1F)

ET1-1 (44) 15:00-15:15
An Energy Efficient Finite State Machine Algorithm for Real-Time Asset Monitoring and Tracking System
Jeongho Lee, Jungkeun Park, and Ki-Duk Kim
C&Tech, Korea

ET1-2 (192) 15:15-15:30
An Accurate and Efficient Stochastic Computing Adder Exploiting Bit Shuffle Control Scheme
Donghui Lee, Junhyuk Baik, and Yongtae Kim
Kyungpook National University, Korea

ET1-3 (129) 15:30-15:45
Correlation Aware Random Pattern Generation for Test Time and Shift Power Reduction of Logic BIST
Jongho Park, Sangjun Lee, Inhwan Lee, Sungwhan Park, and Sungho Kang
Yonsei University, Korea

ET1-4 (198) 15:45-16:00
A Method for Implementing LSTM-Based Multiple-People Identification System for Non-Contact Health Monitoring on Small-Scale FPGA
Masanao Okamoto, Toshiyuki Inoue, Akira Tsuchiya, and Keiji Kishine
The University of Shiga Prefecture, Japan

ET1-5 (194) 16:00-16:15
A Novel Efficient Approximate Adder Design using Single Input Pair based Computation
Hyelin Seok, Hyoju Seo, Jungwon Lee, and Yongtae Kim
Kyungpook National University, Korea

ETRI Session

DCAS3 Digital Signal Processing

Chair | Kyungsoo Byun *(Pohang University of Science and Technology(POSTECH), Korea)*

16:45~18:00, THURSDAY_OCTOBER 20, 2022
Sandpine (Convention 1F)

DCAS3-1 (107)
16:45-17:00

Hardware-Efficient Barrel Shifter Design Using Customized Dynamic Logic Based MUX

Dain Chon, Yoojeong Yang, Hayoung Choi, and Woong Choi

Sookmyung Women's University, Korea

DCAS3-2 (20)
17:00-17:15

Reconfigurable Stochastic Computing Architecture for Computationally Intensive Applications

Jeongeun Kim, Yue Ri Jeong, Kwonneung Cho, Won Sik Jeong, and Seung Eun Lee

Seoul National University of Science and Technology, Korea

DCAS3-3 (143)
17:15-17:30

Low-Complexity High-Performance Method for Calculating Arbitrary Logarithm Function

Yongzhen Zhang[1], Yuan Zhang[2], Yonggang Zhang[3], and Hui Chen[3]

[1]Zhengzhou University, China
[2]Shanghai University of Engineering Science, China
[3]Nanjing University, China

DCAS3-4 (227)
17:30-17:45

Hardware Design of Optimized Large Integer Schoolbook Polynomial Multiplications on FPGA

Monalisa Das and Babita Jajodia

Indian Institute of Information Technology, India

DCAS3-5 (45)
17:45-18:00

A Cost-efficient FPGA-based Embedded System for Biosensor Platform

Iksu Jang, Jaeyoung Seo, Changjae Moon, and Byungsub Kim

Pohang University of Science and Technology (POSTECH), Korea

ORAL SESSIONS

OPENEDGES Technology Session

ML1 Novel Algorithms for AI

Chair | Jaeha Kung *(Daegu Gyeongbuk Institute of Science & Technology (DGIST), Korea)*

16:45~18:00, THURSDAY_OCTOBER 20, 2022
Cheon-Yeon (Reception B1F)

ML1-1 (217) 16:45-17:00
A Morphological Image-based Recognition of Iron Triad using a Convolutional Neural Network
Evelyn Q. Raguindin[1], Reibelle Q. Raguindin[2], Mark Angelo C. Purio[1,3], and Ronnie O. Serfa Juan[4]
[1]Adamson University, Philippines
[2]Hanyang University, Korea
[3]Kyushu Institute of Technology, Japan
[4]Kyungpook National University, Korea

ML1-2 (229) 17:00-17:15
Channel-Wise Activation Map Pruning using Max- Pool for Reducing Memory Accesses
Han Cho and Jongsun Park
Korea University, Korea

ML1-3 (262) 17:15-17:30
Percentile Clipping based Low Bit-Precision Quantization for Depth Estimation Network
Seungeon Hwang and Jongsun Park
Korea University, Korea

ML1-4 (154) 17:30-17:45
Feature Distribution-based Knowledge Distillation for Deep Neural Networks
Hyeonseok Hong and Hyun Kim
Seoul National University of Science and Technology, Korea

ML1-5 (207) 17:45-18:00
ApproxTorch: An Approximate Multiplier Evaluation Environment for CNNs based on Pytorch
Ke Ma and Shinji Kimura
Waseda University, Japan

Samsung Session

DCAS4 Hardware Security Circuits

Chair | Won-Young Lee *(Seoul National University of Science and Technology, Korea)*

08:30~09:45, FRIDAY_OCTOBER 21, 2022
Sandpine (Convention 1F)

DCAS4-1 (118) 08:30-08:45
A 3.65 Gb/s Area-Efficiency ChaCha20 Cryptocore
Ronaldo Serrano, Marco Sarmiento, Ckristian Duran, Trong-Thuc Hoang, and Cong-Kha Pham
The University of Electro-Communications (UEC), Japan

DCAS4-2 (197) 08:45-09:00
FPGA Implementation of Hybrid Karatsuba Multiplications for NIST Post-Quantum Cryptographic Hardware Primitives
Monalisa Das and Babita Jajodia
Indian Institute of Information Technology, India

DCAS4-3 (238) 09:00-09:15
Kyber Accelerator on FPGA Using Energy-Efficient LUT-Based Barrett Reduction
Da Won Kim, Dalta Imam Maulana, and Wanyeong Jung
Korea Advanced Institute of Science and Technology(KAIST), Korea

DCAS4-4 (15) 09:15-09:30
An Extremely Light-Weight Countermeasure to Power Analysis Attack in Dedicated Circuit for AES
Yui Koyanagi and Tomoaki Ukezono
Fukuoka University, Japan

DCAS4-5 (189) 09:30-09:45
A Novel Ring Oscillator PUF for FPGA Based on Feedforward Ring Oscillators
Tuan-Kiet Dang, Ronaldo Serrano, Trong-Thuc Hoang, and Cong-Kha Pham
University of Electro-Communications (UEC), Japan

ORAL SESSIONS

MetaCNI Session

ML2 Circuits to Systems for AI

Chair | Taigon Song *(Kyungpook National University, Korea)*

08:30~09:45, FRIDAY_OCTOBER 21, 2022
Cheon-Yeon (Reception B1F)

ML2-1 (56)
08:30-08:45

Real-time Implementation of 11-key Pose Estimation for Driver Behavior Analysis

Minjoon Kim, Jaehyuk So, and Taemin Hwang

Korea Electronics Technology Institute(KETI), Korea

ML2-2 (203)
08:45-09:00

Backward Graph Construction and Lowering in DL Compiler for Model Training on AI Accelerators

Hyunjeong Kwon, Youngsu Kwon, and Jinho Han

Electronics and Telecommunications Research Institute (ETRI), Korea

ML2-3 (33)
09:00-09:15

^2b-sigmoid and ^2b-tanh: Low Hardware Complexity Activation Functions for LSTM

Yuan Zhang[1], Lele Peng[1], Lianghua Quan[2], Shubin Zheng[1], Qiufeng Feng[1], Yonggang Zhang[2], and Hui Chen[2]

[1]Shanghai University of Engineering Science, China
[2]Nanjing University, China

ML2-4 (82)
09:15-09:30

An FPGA Implementation of CNN-based Compression Artifact Reduction

Jaemyung Kim[1], Jin-Ku Kang[1], and Yongwoo Kim[2]

[1]Inha University, Korea
[2]Sangmyung University, Korea

ML2-5 (223)
09:30-09:45

A Layer-wise Training and Pruning Method for Memory Efficient On-chip Learning Hardware

Dongwoo Lew and Jongsun Park

Korea University, Korea

Synopsys Session

DCAS5 Communication Circuits and Systems

Chair | Byeong Yong Kong *(Kongju National University, Korea)*

14:00~15:15, FRIDAY_OCTOBER 21, 2022
Sandpine (Convention 1F)

DCAS5-1 (153) 14:00-14:15
Hardware Analysis of Channel Estimation Method for IRS-Aided MIMO Wireless Systems
Jiwon Kim, Seungsik Moon, and Youngjoo Lee
Pohang University of Science and Technology(POSTECH), Korea

DCAS5-2 (121) 14:15-14:30
Smart Computational Resource Distribution System with Automatic Classification Interface for CPS
Yuuki Teramura, Toshiyuki Inoue, Akira Tsuchiya, and Keiji Kishine
The University of Shiga Prefecture, Japan

DCAS5-3 (174) 14:30-14:45
Data Bus Inversion Encoding for Improving the Power Efficiency of SERDES-Containing Data Bus
Seongyoon Kang and Jongsun Park
Korea University, Korea

DCAS5-4 (239) 14:45-15:00
Low-Complexity Architecture of Finding First Four Minimum Values for Non-binary LDPC Decoders
Thang Xuan Pham[1], Phap Duong-Ngoc[1], Hanho Lee[1], and Tuy Tan Nguyen[2]
[1]Inha University, Korea
[2]Northern Arizona University, USA

DCAS5-5 (68) 15:00-15:15
An electrical chromatic dispersion emulator using digital signal processing
Koki Ando, Yukinaga Shimoda, Daisuke Ito, and Makoto Nakamura
Gifu University, Japan

ORAL SESSIONS

OPENEDGES Technology Session

RF | Advanced Radio-Frequency Design Techniques

Chair | Jusung Kim *(Hanbat National University, Korea)*

14:00~15:15, FRIDAY_OCTOBER 21, 2022
Cheon-Yeon (Reception B1F)

RF-1 (232) 14:00-14:15
A Ka band FMCW Transmitter with a High Ratio Multiplier
Junho Moon, Sukwon Kang, Dongyeol Yang, and Byung-Sung Kim
Sungkyunkwan University, Korea

RF-2 (165) 14:15-14:30
A Design of a 50 dB Wide Dynamic Range Digtal Power Amplifier with 0.5 dB Fine Tuning Gain Steps for NB-IoT Transmitter
Myeong Gwan Kim, Gi Sung Jang, and Kang Yoon Lee
SKAIChips, Korea

RF-3 (164) 14:30-14:45
Dual Band Wide Range PLL for IoT Application
Ho Won Kim, Hun Park, and Kang Yoon Lee
SKAIChips, Korea

RF-4 (160) 14:45-15:00
***D*-band Power Amplifier Module with Medium Output Power Using *E*-plane Waveguide Transition**
Youngchae Jeon, Jaehoon Jeong, Yeongmin Jang, and Jinho Jeong
Sogang University, Korea

RF-5 (51) 15:00-15:15
Tone-based Measurement of Excess Group Delay in Programmable Gain Receiver Chains for RF Ranging
Ealwan Lee
GCT Semiconductor, Inc., Korea

Telechips Session

SoC2 Design Infrastructure

Chair | Woong Choi *(Sookmyung Women's University, Korea)*

14:00~15:15, FRIDAY_OCTOBER 21, 2022
Ho-Hae (Tower 5 B1F)

SoC2-1 (3) 14:00-14:15
Analysis of Impacting Multi-stack Standard Cells on Chip Implementation
Kyungjoon Chang and Taewhan Kim
Seoul National University, Korea

SoC2-2 (88) 14:15-14:30
Cell-Aware Scan Diagnosis Using Partially Synchronous Set and Reset
Hyeonchan Lim, Hyojoon Yun, Juyong Lee, and Sungho Kang
Yonsei University, Korea

SoC2-3 (219) 14:30-14:45
Performance Variability Modeling of Analog Circuits Using Improved Orthogonal Matching Pursuit
Hyunjun Park and Woo-Seok Choi
Seoul National University, Korea

SoC2-4 (243) 14:45-15:00
Determining PCIe5 Jitter Margin using SIPI Co-Sim
Fern Nee Tan, Li Wern Chew, Sze Lin Mak, Chee Hoong Mah, and Ling Li Ong
Intel Corporation, Malaysia

ORAL SESSIONS

PIXELPLUS Session

ML3 Near-Memory and Special Hardware for AI

Chair | Won-Young Lee *(Seoul National University of Science and Technology, Korea)*

15:45~17:00, FRIDAY_OCTOBER 21, 2022
Sandpine (Convention 1F)

ML3-1 (139) 15:45-16:00
A Novel Processing Unit and Architecture for Process-In Memory (PIM) in NAND Flash Memory
HyunWoo Kim, Seungwon Baek, Jaehong Song, and Taigon Song
Kyungpook National University, Korea

ML3-2 (181) 16:00-16:15
The Quantitative Comparisons of Analog and Digital SRAM Compute-In-Memories for Deep Neural Network Applications
Joonhyung Kim and Jongsun Park
Korea University, Korea

ML3-3 (76) 16:15-16:30
A High-Performance, Low-Power 8-Bit Full-Adder Using 8+T Differential SRAM for Computation-in-Memory
Jihyung Jung and Youngmin Kim
Hongik University, Korea

ML3-4 (195) 16:30-16:45
Performance Analysis of a Phase-Change Memory System on Various CNN Inference Workloads
Jihoon Jang[1], Hyun Kim[1], and Hyokeun Lee[2]
[1]Seoul National University of Science and Technology, Korea
[2]Seoul National University, Korea

ML3-5 (18) 16:45-17:00
Noise-aware and Lightweight LSTM for Keyword Spotting Applications
Yingfeng Wang[1,2], Yi Sheng Chong[1,2], Wang Ling Goh[1], Anh Tuan Do[2]
[1]Nanyang Technological University, Singapore
*[2]A*STAR, Singapore*

TechwidU Session

WLN **Wireline**

Chair | Dong-Woo Jee *(Ajou University, Korea)*

15:45~17:00, FRIDAY_OCTOBER 21, 2022
Cheon-Yeon (Reception B1F)

WLN-1 (42) 15:45-16:00
A Wide Range Digitally Controlled Oscillator with Direct Proportional Loop Control
Yoon Heo and Won-Young Lee
Seoul National University of Science and Technology, Korea

WLN-2 (29) 16:00-16:15
A 5GHz All-Digital PLL with shunt regulating Ring DCO in BOST for DDR5 ATE
Kyungmin Baek, Kahyun Kim, and Deog-Kyoon Jeong
Seoul National University, Korea

WLN-3 (190) 16:15-16:30
Impact of PI Nonlinearity on High-Resolution Frequency-to-Digital Converter
Honggyoo Ahn, Joonghyun Song, and Woo-Seok Choi
Seoul National University, Korea

WLN-4 (55) 16:30-16:45
A Low-Power Counter-based Digital CDR
Hyun-In Kim and Jin-Ku Kang
Inha University, Korea

WLN-5 (52) 16:45-17:00
An Wide-range Low Power Quarter Rate Single Loop CDR
Jin-Ho Kim and Jin-Ku Kang
Inha University, Korea

ABOV Semiconductor Session

ET2 Emerging Technologies for Circuits and Systems

Chair | Yongtae Kim *(Kyungpook National University, Korea)*

15:45~17:00, FRIDAY_OCTOBER 21, 2022
Ho-Hae (Tower 5 B1F)

ET2-1 (148) 15:45-16:00
A 13.56MHz Power-Efficient Active Rectifier for Biomedical Systems
Jisan Ahn, Hyun-Su Lee, and Hyung-Min Lee
Korea University, Korea

ET2-2 (177) 16:00-16:15
Design of Energy Harvesting System with Piezoelectric Device for Onetime-High-Energy Applications
Yoonho Song, Eunseo Kim, and Deog-Kyoon Jeong
Seoul National University, Korea

ET2-3 (233) 16:15-16:30
2T Neuromorphic Device based on oxide semiconductor with High Linearity and Symmetry for High-Precision Training
Seongmin Park, Gilsu Jeon, Suwon Seong, and Yoonyoung Chung
Pohang University of Science and Technology(POSTECH), Korea

ET2-4 (150) 16:30-16:45
A Charge-Controlled Neural Stimulation System for Implantable Devices
Minju Park and Hyung-Min Lee
Korea University, Korea

ET2-5 (241) 16:45-17:00
A 1.92 µA Always-on ECG Monitoring Mixed-Signal SoC for Implantable Medical Application
Syed Muhammad Abubakar[1], Hanjun Jiang[1,2], Yue Yin[1], Jiahua Shi[1], Xiaofeng Yang[2], Wen Jia[2], and Zhihua Wang[1,2]
[1]Tsinghua University, China
[2]Research Institute of Tsinghua University in Shenzhen, China

Samsung Session

SS1 Design and Testing Techniques for Computing-In-Memories

Organizer: Prof. Yu-Guang Chen *(National Central University, Taiwan)*

Abstract: Computing-In-Memories is a promising approach to overcome Von Neumann Bottleneck in computer system when running data-intensive applications. By slightly modifying the structure and peripheral circuits, the logic and arithmetic computations can be done directly in the memory, which significantly improves the performance. Various Computing-In-Memory architectures as well as operation techniques have been addressed recently for various applications, especially neural network computations. However, the CIM suffers from threats of reliability issues due to the vulnerable essence. Therefore, it is important to provide appropriate testing and tolerance techniques. In this session, four papers will discuss the designing and testing techniques for Computing-In-Memories. The first paper provides a brief tutorial on computing-in-memory (CIM) designs and test techniques, and the second paper propose a novel higher precision dot multiplication engine for MAC operations. The third paper gives an aging-aware in-memory computing framework to tolerance aging-induced reliability degradation, while the fourth paper shows a synaptic array and weight mapping method for DNNs.

Chair | Yu-Guang Chen *(Ritsumeikan University, Japan)*

13:00~14:15, WEDNESDAY_OCTOBER 19, 2022
Ho-Hae (Tower 5 B1F)

SS1-1 (125) 13:00-13:15
Design and Test of Computing-In Memories
Jin-Fu Li
National Central University, Taiwan

SS1-2 (61) 13:15-13:30
Design and Dataflow for Multibit SRAM-Based MAC Operations
Chuan-Han Cheng[1], Shih-Hsu Huang[1], and Jin-Fu Li[2]
[1]*Chung Yuan Christian University, Taiwan*
[2]*National Central University, Taiwan*

SS1-3 (98) 13:30-13:45
An Aging Detection and Tolerance Framework for 8T SRAM Dot Product CIM Engine
Yu-Guang Chen[1], Chi-Hsu Wang[1], and Ing-chao Lin[2]
[1]*National Central University, Taiwan*
[2]*National Cheng Kung University, Taiwan*

SS1-4 (71) 13:45-14:00
Layer-wise Exploration of Synaptic Array and Weight Mapping on Heterogeneous Tile-based RRAM CIM Architecture
Hsin-Tzu Wu, Hsin-Yi Pai, and Wei-Kai Cheng
Chung Yuan Christian University, Taiwan

SPECIAL SESSIONS

Synopsys Session

SS2 Memory-Centric Accelerator Design for Deep Neural Network Applications

Organizer: Prof. Po-Tsang Huang *(National Yang Ming Chiao Tung University, Taiwan)*
Prof. Yung Du *(Nanjing University, China)*

Abstract: Deep neural networks (DNN) are widely used in feature classification, object detection, recommender system and so on. Moreover, graph neural networks (GNNs) appear to be a powerful approach to analyzing non-Euclidean data structures and achieving unprecedented performance on graph processing tasks. Unfortueately, DNNs and GNNs are both memory-intensive and computation-intensive, and data accesses and movements dominate the overall energy efficiency by matrix computations and ff-chip memory accesses. In this special session, therefore, memory-centric computing and accelerator design will be discussed to reduce off-chip memory accesses from the aspects of algorithms, architectures, and circuits, particularly emphasizing on the design techniques of data reuse, workload mapping, dataflow, and computation-in-memory circuits.

Chair | Po-Tsang Huang *(National Yang Ming Chiao Tung University, Taiwan)*
Yung Du *(Nanjing University, China)*

13:00~14:15, WEDNESDAY_OCTOBER 19, 2022
Hae-Woon (Tower 5 B1F)

SS2-1 (10) 13:00-13:15
SVR: A Shard-aware Vertex Reordering Method for Efficient GNN Execution and Memory Access
Xingyuan Hu, Zhuang Shao, Chenjia Xie, Li Du, and Yuan Du
Nanjing University, China

SS2-2 (81) 13:15-13:30
Roadmap for Ferroelectric Memory: Challenges and Opportunities for IMC Applications
Sourav De, Maximilian Lederer, Yannick Raffel, Franz Müller, Konrad Seidel, and Thomas Kämpfe
Fraunhofer-Institut für Photonische Mikrosysteme, Germany

SS2-3 (123) 13:30-13:45
Memory-Centric Fusion-based CNN Accelerator with 3D-NoC and 3D-DRAM
Wei Lu, Pei-Yu Ge, Po-Tsang Huang, Hung-Ming Chen, and Wei Hwang
National Yang Ming Chiao Tung University, Taiwan

SS2-4 (124) 13:45-14:00
Precision-Aware Workload Distribution and Dataflow for a Hybrid Digital-CIM Deep CNN Accelerator
Jui-I Kao, Wei Lu, Po-Tsang Huang, and Hung-Ming Chen
National Yang Ming Chiao Tung University, Taiwan

SS2-5 (134) 14:00-14:15
Lego: Dynamic Tensor-Splitting Multi-Tenant DNN Models on Multi-Chip-Module Architecture
Zhou Yu Xuan, Ching-Jul Lee, and Tsung Tai Yeh
National Yang Ming Chiao Tung University, Taiwan

DB HiTek Session

SS3 Algorithm-or Architecture-Level Schemes for Reducing Operation Complexity of Neural Networks

Organizer: Prof. Xin Lou *(SanghaiTech University, China)*
Prof. Song-Nien Tang *(Chung Yuan Christian University, Taiwan)*

Abstract: Recently, neural network schemes based on deep learning technology have been widely used in many fields for artificial intelligence (AI) applications. To increase the execution speed of edge AI devices, it has become a trend that the hardware acceleration schemes have been applied to the neural network inference implementation. In such a development, the reduction of hardware costs and power consumption is an important issue. For this issue, the simplification of neural network inference operations is an effective approach and both algorithmic and hardware architectural solutions can be considered. In this proposal, we plan to explore and propose suitable schemes in the algorithm or architecture level aiming to reduce the operation complexity of neural networks. We expect the proposed works lend support to area- and energy-efficiency improvements in the hardware acceleration design for the neural network inference implementation.

Chair | Xin Lou *(SanghaiTech University, China)*
Song-Nien Tang *(Chung Yuan Christian University, Taiwan)*

14:30~15:45, WEDNESDAY_OCTOBER 19, 2022
Ho-Hae (Tower 5 B1F)

SS3-1 (67) 14:30-14:45
Dataflow and Hardware Design for The Sharing of Feature Maps
De-Yang Chiu and Shih-Hsu Huang
Chung Yuan Christian University, Taiwan

SS3-2 (86) 14:45-15:00
High Accuracy Abnormal ECG Detection Chip Using a Simple Neural Network
Kai-Fen Chang[1] and Yuan-Ho Chen[1,2]
[1]Chang Gung University, Taiwan
[2]Chang Gung Memorial Hospital, Taiwan

SS3-3 (115) 15:00-15:15
Long-Length Accumulation Unit with Efficient Biasing for Binary Weight CNNs
Song-Nien Tang and Chu-Ming Yen
Chung Yuan Christian University, Taiwan

SS3-4 (187) 15:15-15:30
A Machine Learning Accelerator for DDoS Attack Detection and Classification on FPGA
Yu-Kuen Lai, Kai-Po Chang, Xiu-Wen Ku, and Hsiang-Lun Hua
Chung-Yuan Christian University, Taiwan

SS3-5 (209) 15:30-15:45
A Multi-precision Multiply-Accumulation Array
Chaolin Rao, Yueyang Zheng, and Haochuan Wan
ShanghaiTech University, China

SPECIAL SESSIONS

ETRI Session

SS4 Design, Analysis and Tools for Integrated Circuits and Systems (DATICS)

Organizer: Prof. Ka Lok Man *(Xi'an Jiaotong-Liverpool Unversity, China)*

Abstract: DATICS workshops/special sessions were initially created by a network of researchers and engineers both from academia and industry in the areas of Design, Analysis and Tools for Integrated Circuits and Systems (DATICS). The proposed DATICS-ISOCC'22 special session will focus on emerging Circuits and Systems (CAS) topics that will strongly lead human life revolutions, especially in CMOS technologies, communication technologies and biomedical technologies. Human life revolutions come along with economic opportunities. The market for these emerging topics is also forecast to grow to a multi-billion dollar market in the coming decade.
The special session will highlight the potential and current developments of these CAS topics, along with pressing challenges. The proposed session is coherent and complementary to the conference theme and areas of interest of ISOCC. The main target of DATICS-ISOCC'22 is to bring together engineering researchers and people from industry to exchange theories, ideas, techniques and experiences.

Chair | Ka Lok Man *(Xi'an Jiaotong-Liverpool Unversity, China)*

14:30~15:45, WEDNESDAY_OCTOBER 19, 2022
Hae-Woon (Tower 5 B1F)

SS4-1 (96) 14:30-14:45
Spiking Neural Networks for digital hand-written number recognition
Dian Sheng[1], Rongxuan Xu[1], Qinan Wang[1,2], and Chun Zhao[1,2]
[1]*Xi'an Jiaotong-Liverpool University, China*
[2]*University of Liverpool, UK.*

SS4-2 (119) 14:45-15:00
Neuromorphic Hardware Based on Artificial Synaptic Devices
J Li[1,2], C Zhao[1,2], and K Man[1]
[1]*Xi'an Jiaotong-Liverpool University, China*
[2]*University of Liverpool, UK*

SS4-3 (126) 15:00-15:15
Digital Twin based Maximum Power Point Estimation of Photovoltaic Systems
Kangshi Wang[1,2], Jieming Ma[1], Jingyi Wang[1], Bo Xu[1], Yifan Tao[1], and Ka Lok Man[1]
[1]*Xi'an Jiaotong-Liverpool University, China*
[2]*University of Liverpool, UK*

SS4-4 (131) 15:15-15:30
A Long-Term Synchronized System for Healthcare
Gianfranco Avitabile[1], Antonello Florio[1], Ka Lok Man[2], and Chun Zhao[2]
[1]*Polytechnic University of Bari, Italy*
[2]*Xi'an Jiaotong-Liverpool University, China*

SS4-5 (132) 15:30-15:45
Estimating the Angle of Arrival from Multiple RF Sources using Phase Interferometry
Antonello Florio[1], Gianfranco Avitabile[1], and Ka Lok Man[2]
[1]*Polytechnic University of Bari, Italy*
[2]*Xi'an Jiaotong-Liverpool University, China*

KETI Session

SS5 Emerging Applications and FPGA Implementation of Machine Learning

Organizer: Prof. Hiroyuki Tomiyama *(Ritsumeikan University, Japan)*
Prof. Hiroki Nishikawa *(Osaka University, Japan)*

Abstract: Artificial intelligence based on machine learning is now a fundamental part of the social infrastructure that supports our daily lives, and the application fields of machine learning are rapidly expanding. Machine learning is a general-purpose technology, but optimizing internal structures and algorithms for each application is necessary to achieve high inference accuracy. Furthermore, in order to reduce learning or inference time while keeping a high degree of flexibility and scalability, FPGA implementation, rather than CPUs or GPUs, is more effective.
This special session invites six papers on emerging applications and FPGA implementation of machine learning. The first five papers describe machine learning technologies for emerging applications such as energy management, autonomous drones, abnormal event detection, spy photography prevention and human detection. The last paper presents an efficient FPGA implementation of machine learning.

Chair | Hiroyuki Tomiyama *(Ritsumeikan University, Japan)*
Hiroki Nishikawa *(Osaka University, Japan)*

16:00~17:30, WEDNESDAY_OCTOBER 19, 2022
Ho-Hae (Tower 5 B1F)

SS5-1 (43) 16:00-16:15
An Evaluation of Electricity Demand Forecasting Models for Smart Energy Management Systems
Naoya Kaneko, Koki Iwabuchi, Kenshiro Kato, Daichi Watari, Dafang Zhao, Ittetsu Taniguchi, Hiroki Nishikawa, and Takao Onoye
Osaka University, Japan

SS5-2 (27) 16:15-16:30
Monocular Depth Estimation with Optical Flow Attention for Autonomous Drones
Tomoyasu Shimhada[1], Hiroki Nishikawa[2], Xiangbo Kong[1], and Hiroyuki Tomiyama[1]
[1]Ritsumeikan University, Japan
[2]Osaka University, Japan

SS5-3 (145) 16:30-16:45
Joint Generative Network for Abnormal Event Detection in Surveillance Videos
Savath Saypadith[1], Sunepha Detvongsa[2], and Takao Onoye[3]
[1]National University of Laos, Laos
[2]iQURi Tech Company Limited, Laos
[3]Osaka University, Japan

SS5-4 (105) 16:45-17:00
Implementation of AI characteristic motion detecting for improper-photography prevention system
Yusuke Inoue, Xiangbo Kong, and Takeshi Kumaki
Ritsumeikan University, Japan

SPECIAL SESSIONS

SS5-5 (38)
17:00-17:15

Fusing Infrared and Visible Images for DNN-based Nighttime Human Detection

Wanyin Shi[1], Hiroki Matsumiya[1], Hiroki Nishikawa[2], Xiangbo Kong[1], and Hiroyuki Tomiyama[1]
[1]*Ritsumeikan University, Japan*
[2]*Osaka University, Japan*

SS5-6 (32)
17:15-17:30

CNN Acceleration based on Dynamic Pruning and FPGAs Implementation

Qi Li, Hengyi Li, and Lin Meng
Ritsumeikan University, Japan

PIXELPLUS Session

SS6 Hardware Security, Reliability and Trust for SoCs

Organizer: Dr. Zhao Huang *(Xidian University, China)*
Dr. MD Tanvir Arafin *(George Mason University, USA)*

Abstract: System-on-Chip (SoC) chip is the important component of social and personal information systems, which has currently dominated in the end-application market. However, with the development of modern SoC technology and the ubiquity of SoC-based computing devices connected via network, the security, reliability and trust of SoCs have become a pressing issue during the past decade. Since the end product of SoC requires the cooperation from third-party (3P) intellectual property (IP) core vendors, commercial electronic design automation (EDA) companies and offshore foundries, any part of this global business model can be an entry point for hackers to launch various attacks. For example, an adversary may insert Hardware Trojan (HT) into SoC/IP design, develop SoCs using untrusted EDA tools, malicious integrate untrusted 3PIP, overbuild SoC chips, etc. All of these hardware-based issues will significantly affect the security, reliability and trust of SoC chips. Given this situation, it is both critical and challenging to study defensive strategies to alleviate these potential security threats.
In this Special Session (SS), we will have discussions on the security, reliability and trust of SoCs from various viewpoints. Formal verification, Model Checking, Evolvable Hardware, Reinforcement Learning, optimized SM4 and EDA Tool security are discussed for exploring research directions of secure SoCs.

Chair | Zhao Huang *(Xidian University, China)*
MD Tanvir Arafin *(George Mason University, USA)*

16:00~17:30, WEDNESDAY_OCTOBER 19, 2022
Hae-Woon (Tower 5 B1F)

SS6-1 (89) 16:00-16:15
Accelerating SoC Security Verification and Vulnerability Detection Through Symbolic Execution
Shibo Tang, Xingxin Wang, Yifei Gao, and Wei Hu
Northwestern Polytechnical University, China

SS6-2 (90) 16:15-16:30
Towards Automatic Property Generation for SoC Security Verification
Xingxin Wang, Shibo Tang, and Wei Hu
Northwestern Polytechnical University, China

SS6-3 (34) 16:30-16:45
Exploring the high-throughput and low-delay hardware design of SM4 on FPGA
Yixiao Chen[1], Jinfeng Song[2,3,4], Shuai Chen[5], Yuan Cao[1], Jing Ye[2,3,4], Huawei Li[2,3,4], Xiaowei Li[2,3,4], Xin Lou[6], and Enyi Yao[7]
[1]Hohai University, China
[2]CAS, China
[3]University of Chinese Academy of Sciences, China
[4]CASTEST, China
[5]Binary Semi. Co. Ltd., China
[6]ShanghaiTech University, China
[7]South China University of Tech., China

SPECIAL SESSIONS

SS6-4 (37)
16:45-17:00

Investigate of Mitigation Solution against Hardware Trojans Attack on Evolvable Hardware Platform

Zeyu Li, Zhao Huang, Junjie Wang, and Quan Wang
Xidian University, China

SS6-5 (235)
17:00-17:15

A survey and perspective on electronic design automation tools for ensuring SoC security

Tian Feng[1], Haojie Pei[1], Zhou Jin[1], and Xiao Wu[2]
[1]*China University of Petroleum-Beijing, China*
[2]*Huada Empyrean Software Co. Ltd, China*

SS6-6 (269)
17:15-17:30

Reinforcement Learning for Hardware Security: Opportunities, Developments, and Challenges

Satwik Patnaik, Vasudev Gohil, Hao Guo, and Jeyavijayan (JV) Rajendran
Texas A&M University, USA

NEXTCHIP Session

SS7 Analysis and Design of Power and Energy Circuits and Systems

Organizer: Prof. Yu-Guang Chen *(National Central University, Taiwan)*

Abstract: This session discusses analysis and design of power and energy circuits and systems. The topics of dc-dc converters, wireless power transfer, energy-harvesting circuits, and gate drivers are included in this proposed session. Power energy circuits and systems are becoming increasingly important as awareness of environmental issues grows. The dc-dc converters are required high frequency, small and light scale, and high efficiency. The energy-harvesting and wireless-power-transfer systems are also done, which are now at the stage of looking at practical applications. Because of the high-frequency trend, the gate-driver design is one of the most important issues. This session can discuss the cutting-edge research results around the above problems.

Chair | Hiroo Sekiya *(Chiba University, Japan)*

13:30~14:45, THURSDAY_OCTOBER 20, 2022
Hae-Woon (Tower 5 B1F)

SS7-1 (46) 13:30-13:45
Design of Class-EF^2 WPT System with Relay Coil
Yota Matsui, Kisara Nakajima, Weisen Luo, and Xiuqin Wei
Chiba Institute of Technology, Japan

SS7-2 (49) 13:45-14:00
Chattering phenomenon in a high-side gate driver circuit using MOSFET equivalent circuit
Yusuke Goto[1], Hiroyuki Asahara[2], Daisuke Ito[3], and Takuji Kousaka[1]
[1]Chukyo University, Japan
[2]Okayama University of Science, Japan
[3]Gifu University, Japan

SS7-3 (104) 14:00-14:15
Comparative Study of Nonlinear Dynamics in DC-DC Converter with TEM
Daiki Hozumi[1] , Shota Uchino[3] , Takuji Kousaka[2], and Hiroyuki Asahara[1]
[1]Okayama University of Science, Japan
[2]Chukyo University, Japan
[3]Anan College, Japan

SPECIAL SESSIONS

SS7-4 (111)
14:15-14:30

A simple approach of stability analysis and MPPT control in DC-DC converter with TEM

Yuma Furutani[1] , Takuji Kousaka[2] , Shota Uchino[3], and Hiroyuki Asahara[1]
[1]*Okayama University of Science, Japan*
[2]*Chukyo University, Japan*
[3]*Anan College, Japan*

SS7-5 (112)
14:30-14:45

Maximum Efficiency Tracking for Wireless Power Transfer with Multiple Receivers

Toshihiro Matsuda, Yutaro Komiyama, Wenqi Zhu, Kien Nguyen, and Hiroo Sekiya
Chiba University, Japan

Neowine Session

SS8 Emerging Applications of Intelligent System Semiconductor

Organizer: Prof. Suk-Ju Kang *(Sogang University, Korea)*

Abstract: In this special session, papers on variously applicable systems, circuit designs, and device technologies related to intelligent semiconductors will be presented. Through these papers, we will look at recent technology trends and research directions, and discuss them from various research perspectives.

Chair | Suk-Ju Kang *(Sogang University, Korea)*

15:00~16:15, THURSDAY_OCTOBER 20, 2022
Hae-Woon (Tower 5 B1F)

SS8-1 (13)
15:00-15:15

Performance Comparison of Soiling Detection Using Anomaly Detection Methodology

JungHoon Lee, Chang-Ryeol Jeon, and Suk-Ju Kang

Sogang University, Korea

SS8-2 (65)
15:15-15:30

A High Slew-rate Wide-range Capacitive Load Driving Buffer Amplifier with Correlated Dual Positive Feedback Loops

Young-Ju Oh, Hyo-Jin Park, Joo-Mi Cho, Hyeon-Ji Choi, Su-Min Park, Chan-Ho Lee, Esun Baik, Chan-Kyu Lee, Ho-Chan Ahn, and Sung-Wan Hong

Sogang University, Korea

SS8-3 (127)
15:30-15:45

The effect of CMOS/CFE in MFMIS-based ferroelectric tunnel field-effect transistor (FeTFET)

Hyung Ju Noh, Seungwon Go, and Sangwan Kim

Sogang University, Korea

SS8-4 (158)
15:45-16:00

A 430-MS/s 7-b Asynchronous SAR ADC With a 40 fF Input Sampling Capacitor

Hyoung-Jung Kim[1], Jae-Hyuk Lee[1], Jae-Geun Lim[1], Jun-Ho Boo[1], Ho-Jin Kim[1], Seong-Bo Park[1], Youngdon Choi[2], Jung-Hwan Choi[2], and Gil-Cho Ahn[1]

[1]Sogang University, Korea
[2]Samsung Electronics, Korea

SS8-5 (162)
16:00-16:15

Miniaturization of bandwidth extension circuit for ESD I/O pad using bridged T-coil

Jaehoon Jeong, Hyungeun Kim, Jihyeon Lee, Jaehyun Park, Jongsin Shin, and Jinho Jeong

Sogang University, Korea

SPECIAL SESSIONS

LX Semicon Session

SS9 Low Power Accelerator Design Utilizing Neural Networks for IoT Applications

Organizer: Prof. Tony Tae-Hyoung Kim *(Nanyang Technological University, Singapore)*

Abstract: Recent development of Artificial Intelligence (AI) and Machine Learning (ML) have driven the progress in accelerator design based on neural networks. While deep neural networks (DNNs) have demonstrated substantial advantages in various domains, small-scale neural networks have also attracted research interest because of edge computing where energy efficiency and hardware complexity are significant design constraints. In this special session, various low power accelerators for edge computing based on neural networks will be presented. Several accelerators with different architectures and target applications will be discussed to address the limitations of DNNs for edge computing or IoT applications.

Chair | Tony Tae-Hyoung Kim *(Nanyang Technological University, Singapore)*

16:45~18:00, THURSDAY_OCTOBER 20, 2022
Ho-Hae (Tower 5 B1F)

SS9-1 (47) 16:45-17:00
A Robust and Lightweight Environmental Sound Classification Technique with Adaptation to Microphone for AIoT Sound Sensing
Lujie Peng, Longke Yan, Junyu Yang, Zhiyi Chen, and Jun Zhou
University of Electronic Science and Technology of China, China

SS9-2 (58) 17:00-17:15
A Neuromorphic SLAM Accelerator Supporting Multi-Agent Error Correction in Swarm Robotics
Jaehyun Lee and Jong-Hyeok Yoon
Daegu Gyeongbuk Institute of Science and Technology (DGIST), Korea

SS9-3 (199) 17:15-17:30
Network-on-Chip-Centric Accelerator Architectures for Edge AI Computing
Bo Wang[1], Ke Dong[1], Nurul Akhira Binte Zakaria[1], Mohit Upadhyay[2], Weng-Fai Wong[2], and Li-Shiuan Peh[2]
[1]*Singapore University of Technology and Design, Singapore*
[2]*National University of Singapore, Singapore*

SS9-4 (41) 17:30-17:45
A Low-Power Gesture Recognition System utilizing Hybrid Tiny Classifiers
Yuncheng Lu, Zehao Li, Xin Zhang, and Tony Tae-Hyoung Kim
Nanyang Technological University, Singapore

Daegu Technopark Session

SS10 Emerging techniques for neural networks, non-linear, and bio-related circuits and systems

Organizer: Prof. Kyeong-Sik Min *(Kookmin University, Korea)*
Prof. Fernando Corinto *(Politecnico di Torino, Italy)*

Abstract: Computer vision technologies are widely used in various applications nowadays. Circuits and systems are needed to support these vision technologies. This session will focus on the design circuits and systems for vision application, including algorithm, architecture, circuits, etc.

Chair | Kyeong-Sik Min *(Kookmin University, Korea)*
Fernando Corinto *(Politecnico di Torino, Italy)*

16:45~18:00, THURSDAY_OCTOBER 20, 2022
Hae-Woon (Tower 5 B1F)

SS10-1 (178) 16:45-17:00
Clustering in Globally Coupled Chaotic Circuits with Changing Weights
Yoko Uwate and Yoshifumi Nishio
Tokushima University, Japan

SS10-2 (236) 17:00-17:15
A Mathematical Analysis of Wire Resistance Problem in Memristor Crossbars
G. Zoppo[1], F. Marrone[1], F. Corinto[1], A. Korkmaz[2], Su–in Yi[2], S. Palermo[2], and R. S. Williams[2]
[1]Politecnico di Torino, Italy
[2]Texas A&M University, USA

SS10-3 (265) 17:15-17:30
Memristor Crossbars for Implementing Convolutional Neural Networks
Jiyong An, Seokjin Oh, and Kyeong-Sik Min
Kookmin University, Korea

SS10-4 (270) 17:30-17:45
Low power Embedded RRAM Array for AI Application
Liang Chang[1], Yi Tong[2], Qiang Wu[3], and Jun Zhou[1]
[1]University of Electronic Science and Technology of China, China
[2]Gusu Laboratory of Materials, China
[3]HOUMO.AI, China

SS10-5 (271) 17:45-18:00
Real-Time Ultrasound Imaging System for Drone Applications
Jerald Yoo
National University of Singapore, Singapore

DEEPX Session

SS11 Circuits and Systems of Artificial Intelligence and Security

Organizer: Prof. Hanho Lee *(Inha University, Korea)*

Abstract: Artificial intelligence (AI) and security are playing an increasingly crucial role in the IoT, 5G/6G, and autonomous mobility applications, and they have also become the fundamental components of modern intelligent society. The applications of AI and security for IoT, 5G/6G and autonomous mobility need to be portable, lightweight, low-latency and high-speed to provide reliable service. Meanwhile, massive devices connected to the edge of communication networks should be post-quantum safe and secure, because emerging quantum computers can easily crack the traditional public-key ciphers. To meet the requirements of high-throughput and diverse application scenarios of next-generation communications and autonomous mobility, it is necessary to resort to configurable and low-latency algorithms and architectures of AI and post-quantum cryptography. The high-performance, low-latency domain specific architecture has become a trend of circuits and systems design in the post-Moore era, which can also be applied to the AI and security in a wide range of applications.

Chair | Hanho Lee *(Inha University, Korea)*

08:30~09:45, FRIDAY_OCTOBER 21, 2022
Ho-Hae (Tower 5 B1F)

SS11-1 (147) 08:30-08:45
High-speed serial interface using PWAM signaling scheme
Hwan-Ung Kim and Jin-Ku Kang
Inha University, Korea

SS11-2 (204) 08:45-09:00
An Efficient Systolic Array with Variable Data Precision and Dimension Support
Jaehyeon So and Jong Hwan Ko
Sungkyunkwan University, Korea

SS11-3 (240) 09:00-09:15
Flexible GPU-Based Implementation of Number Theoretic Transform for Homomorphic Encryption
Phap Duong-Ngoc[1], Thang Xuan Pham[1], Hanho Lee[1], and Tuy Tan Nguyen[2]
[1]*Inha University, Korea*
[2]*Northern Arizona University, USA*

SPECIAL SESSIONS

SS11-4 (258) 09:15-09:30
Search-Efficient NAS: Neural Architecture Search for Classification
Amrita Rana and Kyung Ki Kim
Daegu University, Korea

SS11-5 (259) 09:30-09:45
Automation Framework for Digital Circuit Design and Verification
Hayun Bong, Kyungseon Cho, and Yeongkyo Seo
Inha University, Korea

SPECIAL SESSIONS

ASICLAND Session

SS12 Simulation and Analysis for Nonlinear Problems

Organizer: Prof. Yoko Uwate *(Tokushima University, Japan)*

Abstract: The systems that exist in the real world are very high-dimensional and complex, and the most of them are nonlinear systems.
Therefore, the simulation and analysis of nonlinear systems are very important for the future development of engineering applications, especially in the field of SoC.
This special session will present and discuss the following research topics; optimization using chaotic dynamics and bifurcation, auditory models focusing on nonlinear features, and time series classification using neural networks with nonlinear techniques.

Chair | Yoko Uwate *(Tokushima University, Japan)*

08:30~09:45, FRIDAY_OCTOBER 21, 2022
Hae-Woon (Tower 5 B1F)

SS12-1 (24)
08:30-08:45
Pitch-Shift Effects of an Ergodic Sequential Logic Nonlinear Cochlear Model Induced by Three Tones
Yui Kishimoto and Hiroyuki Torikai
Hosei University, Japan

SS12-2 (50)
08:45-09:00
Computation of homoclinic points using particle swarm optimization in 2-dimensional discrete dynamical systems
Tatsumi Makino[1], Yuu Miino[2], Haruna Matsushita[3], and Takuji Kousaka[1]
[1]Chukyo University, Japan
[2]Naruto University of Education, Japan
[3]Kagawa University, Japan

SS12-3 (116)
09:00-09:15
Time Series Analysis with Noise-Mixing Effects Using Neural Networks
Takuya Nakamura, Ryosuke Shimizu, Yoko Uwate, and Yoshufumi Nishio
Tokushima University, Japan

SS12-4 (83)
09:15-09:30
Investigation of the Effect of Adding Random Noise to Noisy Biological Signals on the Classification of Neural Network
Ryosuke Shimizu, Yoko Uwate, and Yoshifumi Nishio
Tokushima University, Japan

SS12-5 (99)
09:30-09:45
Multi-point search method for system identification based on chaotic dynamics
Masashi Tomita and Tadashi Tsubone
Nagaoka University of Technology, Japan

SPECIAL SESSIONS

Anritsu-Korea Session

SS13 Design and Analysis of Nonlinear Circuits and Networks

Organizer: Prof. Yoshifumi Nishio *(Tokushima University, Japan)*

Abstract: In recent years, nonlinear circuits and networks become more and more important, because intelligent and flexible systems for future electronic systems require complex nonlinear circuits and networks.
From the beginning of the 20th century, plenty of design and analysis methods for nonlinear circuits and networks have been developed over 100 years.
However, we need more powerful tools to design low cost power electronic circuits, to analyze large scale complex nonlinear networks, and to realize more intelligent artificial neural networks.
In this special session, 5 papers are invited to show examples of recent works on design and analysis of such nonlinear circuits and networks.

Chair | Yoshifumi Nishio *(Tokushima University, Japan)*

14:00~15:15, FRIDAY_OCTOBER 21, 2022
Hae-Woon (Tower 5 B1F)

SS13-1 (78) 14:00-14:15
A hardware-efficient sequential logic biochemical switch model toward biosystem simulator
Shogo Shirafuji and Hiroyuki Torikai
Hosei University, Japan

SS13-2 (25) 14:15-14:30
A hardware-efficient ergodic sequential logic neuron network for brain prosthetic FPGA
Yuta Shiomi and Hiroyuki Torikai
Hosei University, Japan

SS13-3 (113) 14:30-14:45
Reduction of Processing Time for Wireless Spiking Neural Network Using Wireless Communication Devices for IoT
Ryuji Nagazawa[1], Kien Nguyen[1], Hiroo Sekiya[1], and Hiroyuki Torikai[2]
[1]*Chiba University, Japan*
[2]*Hosei University, Japan*

SS13-4 (85) 14:45-15:00
Synchronization Phenomena of Coupled Oscillators with Node and Edge Weights in Two-Dimensional Complex Networks
Kiichi Yamashita, Yoko Uwate, and Yoshifumi Nishio
Tokushima University, Japan

SS13-5 (106) 15:00-15:15
Phase Change of Three Coupled Chaotic Circuits to Input Signals
Takahiro Hattori, Yoko Uwate, and Yoshifumi Nishio
Tokushima University, Japan

Poster Session

Chair | Seokhyeong Kang *(Pohang University of Science and Technology (POSTECH), Korea)*

Exhibition Time 10:00~17:00, FRIDAY_OCTOBER 21, 2022
Standing Time 15:15~15:45, FRIDAY_OCTOBER 21, 2022
Lakai Ballroom2 (Convention 1F)

Analog Circuits

PS-1 (11) **16 x 10 Pressure Sensor CMOS Driver IC for Resistance Interfence Calibration of Cells**
Jiseong Lee, Seungsoo Kwak, Yun Chan Im, Hyunjin Lee, and Yong Sin Kim
Korea University, Korea

PS-2 (16) **A Novel Study on a 300°C, High Performance LDO Regulator Using Silicon-On-Insulator Process for Extreme Drill Bit Application**
Chiang Liang Kok
Newcastle Australia Institute of Higher Education Pte Ltd, Singapore

PS-3 (36) **STT-MRAM Read and Write Circuit for High Reliability and Power Efficiency**
Dong-Kil Yun and Jung-Hoon Chun
Sungkyunkwan University, Korea

PS-4 (73) **A 80-MHz 91.2 ppm/°C Self-Biased Frequency-Locked-Loop Timer**
Tsung-Ying Chen, Ching-Yuan Yang, and Dung-An Wang
National Chung Hsing University, Taiwan

PS-5 (101) **A Design of SIDITO Buck-Boost Converter with Real Time Maximum Power Point Tracking for RF Energy Harvesting System**
Hyun Jin Jeong and Kang Yoon Lee
Sungkyunkwan University, Korea

POSTER SESSIONS

PS-6 (117) **Capless Low-Dropout Regulator with a Dual Feedback Loop and Voltage Dampers**

Yun Seong Lee, Yun Chan Im, Hyunjin Lee, and Yong Sin Kim

Korea University, Korea

PS-7 (120) **A Three-Level Boost Converter With Peak Current Mode Control for Flying Capacitor Self-Balancing**

Junho Song, Minsu Kim, and Hyung-Min Lee

Korea University, Korea

PS-8 (152) **A Programmable Gain Amplifier with Fast Transient Response for Medical Ultrasound System**

Min-Hyeong Son, Young-Chan Lee, Hyun-Min Baek, Hyo-Jeong Choi, and Ji-Yong Um

Kumoh National Institutue of Technology, Korea

PS-9 (196) **A 12.5-Gb/s Switched Capacitor Based Two Tap DFE With High BER Performance**

Yosep Cho, Jongmin Park, and Jinwook Burm

Sogang University, Korea

Circuits and Systems for Emerging Technologies

PS-10 (12) **A Power-Efficient Low-Noise Neural Recording Amplifier IC with High Tolerance to Stimulation Artifacts**

Soonseong Hong and Hyouk-Kyu Cha

Seoul National University of Science and Technology, Korea

PS-11 (30) **Anomaly information detection and fault tolerance control method for CAN-FD bus network**

Aoran Wang[1], Jie Fang[1], Yinan Xu[1], Yihu Xu[1], Yubing Wang[1], Yujing Wu[1], and Jin-Gyun Chung[2]

[1]YanBian University,China
[2]Jeonbuk National University, Korea

PS-12 (39) **A Biopotential Amplifier IC with Active Common-Mode Cancellation for Closed-Loop Neural Interfaces**

Hyojun Yoo and Hyouk-Kyu Cha

Seoul National University of Science and Technology, Korea

POSTER SESSIONS

PS-13 (77) **Linearity Characterization of Hybrid Driving Scheme for Spatial Light Modulator System**

Z. Di, A. Mani, A. T. Do, A. Baranikov, R. M. Veetil, R. P. Dom´ınguez, A. I. Kuznetsov, and K. T. C. Chai

*A*STAR, Singapore*

PS-14 (245) **Time-Efficient Approximate Stochastic Computing for Medical Imaging Applications**

Keerthana Pamidimukkala[1], Kyung Ki Kim[2], Yong-Bin Kim[3], and Minsu Choi[1]

[1]Missouri Univ of Science & Technology, USA
[2]Daegu University, Korea
[3]Northeastern University, USA

Digital Circuits, Architecture, and Systems

PS-15 (1) **SoC Design for Mobile Real-time Badminton Stroke Classification Design**

Wen-Hsin Tsai and Kuei-Ann Wen

National Yang Ming Chiao Tung University, Taiwan

PS-16 (17) **Adaptive Granularity On-die ECC**

Daero Kim and Jungrae Kim

Sungkyunkwan University, Korea

PS-17 (19) **The first study of 10nm-class backside defect using Co-Routine based ETL in DRAM**

Taesu Shin and Kibum Lee

Samsung Electronics, Korea

PS-18 (28) **Design of State of Charge and Health Estimation for Li-ion Battery Management System**

Minjoon Kim and Jaehyuk So

Korea Electronics Technology Institute(KETI), Korea

PS-19 (74) **Low Power Decoder Architecture of Product Code for Storage Controller**

Sumin Kim, Byungmin Ahn, Bohwan Jun, Mankeun Seo, Hongrak Son, and Yong Ho Song

Samsung Electronics, Korea

POSTER SESSIONS

PS-20 (75) **A Design and Implementation of MIPI A-PHY RTS Layer**

Sang-Ung Shin[1], Jin-Ku Kang[1], and Yongwoo Kim[2]

[1]Inha University, Korea
[2]Sangmyung University, Korea

PS-21 (93) **Automated Reverse Engineering Tools for FPGA Bitstream Extraction and Logic Estimation**

Mannhee Cho[1], Dongchan Lee[2], Sanghyun Lee[2], Youngmin Kim[2], and Hyung-Min Lee[1]

[1]Korea University, Korea
[2]Hongik University, Korea

PS-22 (94) **Data extraction from flash memory and reverse engineering using Xilinx 7 series FPGA boards**

Dongchan Lee[1], Sanghyun Lee[1], Mannhee Cho[2], Hyung-Min Lee[2], and Youngmin Kim[1]

[1]Hongik University, Korea
[2]Korea University, Korea

PS-23 (95) **Defect Detection Circuit Design for CXL Memory**

Junyoung Ko, Jungmin Bak, Changwhi Park, Sangkil Lee, and Jangseok Choi

Samsung Electronics, Korea

PS-24 (137) **Systolic Array based Spiking Neuron Processor with Energy-Efficient Dataflow**

Heetak Kim, Yunpyo Hong, and Taeho Hwang

Korea Electronics Technology Institute(KETI), Korea

PS-25 (159) **Hybrid Assistive Circuit of SRAM for Improving Read and Write Noise Margin in 3nm CMOS**

Jiyoung Lee and Youngmin Kim

Hongik University, Korea

PS-26 (169) **Memory-Access Optimization for Acceleration and Power Saving of FPGA-Based Image Processing**

Shungo Shimohane, Toshiyuki Inoue, Akira Tsuchiya, and Keiji Kishine

The University of Shiga Prefecture, Japan

PS-27 (193) **Releasing the Memory Bottleneck to Display Video Correctly**

Hyeonguk Jang, Sukho Lee, Jae-Jin Lee, and Kyuseung Han

Electronics and Telecommunications Research Institute(ETRI), Korea

POSTER SESSIONS

PS-28 (205) **Logic and Reduction Operation based Hardware Trojans in Digital Design**
Mayukhmali Das, Sounak Dutta, and Sayan Chatterjee
Jadavpur University, India

PS-29 (210) **Tributary SOT-MRAM Cell Structure for Reducing Write Energy**
Yunho Jang and Jongsun Park
Korea University, Korea

PS-30 (246) **A Time-Domain Parallel Counter for Deep Learning Macro**
Yixuan He[1], Minsu Choi[2], Kyung-Ki Kim[3], and Yong-Bin Kim[1]
[1]Northeastern University, USA
[2]Missouri University of Science & Technology, USA
[3]Daegu University, Korea

PS-31 (264) **Design Optimization for Decimation Filter for High Performance Sigma-Delta ADC**
Sang-bo Park, Go-eun Woo, and Hyung Won Kim
Chungbuk National University, Korea

PS-32 (267) **Implementation of Aurora Interface using SFP+ Transceiver**
Sungkyun Shin, Soyeon Choi, Eunchae Lee, Songyeon Lee, and Hoyoung Yoo
Chungnam National University, Korea

Machine Learning and AI

PS-33 (64) **Low Power Ternary XNOR using 10T SRAM for In-Memory Computing**
Sanghyun Lee and Youngmin Kim
Hongik University, Korea

PS-34 (80) **Filter Pruning Method for Inference Time Acceleration Based on YOLOX in Edge Device**
Jihun Jeon[1], Jin-Ku Kang[1], and Yongwoo Kim[2]
[1]Inha University, Korea
[2]Sangmyung University, Korea

PS-35 (87) **Exploring GEMM Operations on Different Configurations of the Gemmini Accelerator**
Dennis A. N. Gookyi, Eunchong Lee, Kyungho Kim, Sung-Joon Jang, and Sang-Seol Lee
Korea Electronics Technology Institute(KETI), Korea

POSTER SESSIONS

PS-36 (109) **Evaluation of Posit Arithmetic on Machine Learning based on Approximate Exponential Functions**

Hyun Woo Oh, Won Sik Jeong, and Seung Eun Lee

Seoul National University of Science and Technology, Korea

PS-37 (110) **ZOS: Zero Overhead Scan for Systolic Array-based AI accelerator**

Jihye Kim[1], Hayoung Lee[2], Jongho Park[2], and Sunho Kang[2]

[1]Samsung Electronics, Korea
[2]Yonsei University, Korea

PS-38 (141) **DNN-based Cancer Recurrence Predictor using FPGA**

Young Jun Lim, Do Young Kim, Joon Hyeon Park, and Myung Hoon Sunwoo

Ajou University, Korea

PS-39 (146) **Impact of Oscillator Phase Noise on Time-Domain SNN Performance**

Jia Park and Woo-Seok Choi

Seoul National University, Korea

PS-40 (149) **Logic Diagnosis Based on Deep Learning for Multiple Faults**

Tae Hyun Kim, Hyeonchan Lim, Minho Cheong, Hyojoon Yun, and Sungho Kang

Yonsei University, Korea

PS-41 (171) **Lightweighted AI-based Inference using Deterministic Randomness Compensation for Microcontroller ADC Resolution Enhancement**

Jisu Kwon and Daejin Park

Kyungpook National University, Korea

PS-42 (226) **Clipped Quantization Aware Training for Hardware Friendly Implementation of Image Classification Networks**

Kyungchul Lee and Jongsun Park

Korea University, Korea

PS-43 (260) **Class Difficulty based Mixed Precision Quantization for Low Complexity CNN Training**

Joongho Jo and Jongsun Park

Korea University, Korea

POSTER SESSIONS

RF/Microwave/Wireless

PS-44 (70) **Electromagnetic Shielding Effectiveness of Sputtered Non-woven Noise Suppression Sheet with Varied Air Gap**

Takumi Nabeshima[1], Daisuke ito[1], Makoto Nakamura[1], Takefumi Koyama[2], and Katsunori Muto[2]

[1]Gifu University, Japan
[2]SEKISUI CHEMICAL CO., LTD., Japan

PS-45 (72) **A 28GHz-band integrated GaAs Power Amplifier for 5G Mobile Communications**

Bonghyuk Park, Hui-Dong Lee, Seunghyun Jang, Sunwoo Kong, Seunghun Wang, and Seok-Bong Hyun

Electronics and Telecommunications Research Institute (ETRI), Korea

PS-46 (151) **A K-band CMOS Power Amplifier with 3-Bit Phase Shifting Characteristics**

Hui Dong Lee, Seunghyun Jang, Sunwoo Kong, Bonghyuk Park, and Seok-Bong Hyun

Electronics and Telecommunications Research Institute (ETRI), Korea

PS-47 (163) **Modified Wilkinson Power Divider with Resonating Stubs for Physical Isolation of Output Ports**

Yeongmin Jang and Jinho Jeong

Sogang University, Korea

SoC Design Methodology and CAD

PS-48 (40) **Enhancement of Emulation Usage for NVMe Solid State Drive**

Jeongbae Seo, Shinbeom Choi, Jaeik Lee, Sekwang Kim, Wooseong Cheong, ByungChul Yoo, and Yong Ho Song

Samsung Electronics, Korea

PS-49 (69) **Toward Heterogeneous Virtual Platforms For Early SW Development**

Dongyoung Lee, Kyungsu Kang, Jongseong Park, Byunghoon Lee, Jinbeom Kim, and Jaewoo Im

Samsung Electronics, Korea

POSTER SESSIONS

PS-50 (166) **High-Level Synthesis Considering Layer Assignment on Timing in 3D-IC**

Myeongwoo Jin[1], Doekkeun Oh[2], and Juho Kim[1]

[1]*Sogang University, Korea*
[2]*Samsung Electronics, Korea*

PS-51 (167) **Delay Impact on Process Variation of Interconnect throughout technology scaling**

Myeongwoo Jin[1], Doekkeun Oh[2], and Juho Kim[1]

[1]*Sogang University, Korea*
[2]*Samsung Electronics, Korea*

PS-52 (188) **XSNN: a System-Level Simulator for Spiking Neural Network with Neuron Circuits and Synapse Devices**

Jeong Woo Min and Jaeha Kim

Seoul National University, Korea

PS-53 (200) **Fast Estimation of NTT/INTT Accelerator Costs for RNS-Based Homomorphic Encryption**

Gyuhyun Jung, Hyeokjun Kwon, Hyunhoon Lee, and Youngjoo Lee

Pohang University of Science and Technology(POSTECH), Korea

PS-54 (242) **Lightweighted Shallow CTS Techniques for Checking Clock Tree Synthesizable Paths in RTL Design Time**

Nayoung Kwon and Daejin Park

Kyungpook National University, Korea

Wireline

PS-55 (9) **A Fast Eye Size Evaluation Method for High Speed Signal**

Hyoseok Song, Kwangmin Kim, Changyoon Han, and Byungsub Kim

Pohang University of Science and Technology(POSTECH), Korea

PS-56 (102) **A Highly Linear Digitally Controlled Delay Line with Reduced Duty Cycle Distortion**

Joonghyun Song and Woo-Seok Choi

Seoul National University, Korea

Organized by IDEC IC DESIGN EDUCATION CENTER

Sponsored by SAMSUNG SK hynix DB HiTek

CDC Oral Session

Chair | Sung-Wan Hong *(Sogang University, Korea)*
Won-Young Lee *(Seoul National University of Science and Technology, Korea)*

08:15~09:30, THURSDAY_OCTOBER 20, 2022
Sandpine (Convention 1F)

CDC-O001 08:15-08:30
An E-band Wideband Transmitter and Receiver for High Data Rate in CMOS
Kyunghwan Kim, Kangseop Lee, Chan-Gyu Choi and Ho-Jin Song
Pohang University of Science and Technology(POSTECH), Korea

CDC-O002 08:30-08:45
Energy-Efficient Neural Network Processor Using Analog-Based In-Memory Computing
Jin-O Seo and Seong Hwan Cho
Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-O003 08:45-09:00
A 97fsrms-Jitter, 8.16GHz Ring-Oscillator Injection-Locked Clock Multiplier with Power-Gating Injection-Locking
Suneui Park, Yuhwan Shin, Jeonghyun Lee, and Jaehyouk Choi
Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-O004 09:00-09:15
A 4.45 msLow-latency 3D Point-cloud-based Neural Network Processor for Hand Pose Estimation in Mobile Devices
Dongseok Im, Sanghoon Kang, Donghyeon Han, and Hoi-Jun Yoo
Korea Advanced Institute of Science and Technology (KAIST), Korea

CHIP DESIGN CONTEST

CDC-O005
09:15-09:30

A Fully Integrated Dual-Output Continuously Scalable-Conversion-Ratio Switched-Capacitor Converter.

Taehyeong Park and Chulwoo Kim

Korea University, Korea

CDC Poster Session

09:30~16:15, THURSDAY_OCTOBER 20, 2022

Lakai Ballroom2 (Convention 1F)

CDC-P001 **An E-band Wideband Transmitter and Receiver for High Data Rate in CMOS**

Kyunghwan Kim, Kangseop Lee, Chan-Gyu Choi and Ho-Jin Song

Pohang University of Science and Technology(POSTECH), Korea

CDC-P002 **mm-Wave Wideband Differential Wilkinson Power Dividerwith 90-Degree Rotational Symmetric Layout**

Seonjeong Park and Songcheol Hong

Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P003 **Energy-Efficient Neural Network Processor Using Analog-Based In-Memory Computing**

Jin-O Seo and Seong Hwan Cho

Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P004 **A 4.45 msLow-latency 3D Point-cloud-based Neural Network Processor for Hand Pose Estimation in Mobile Devices**

Dongseok Im, Sanghoon Kang, Donghyeon Han, and Hoi-Jun Yoo

Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P005 **A Fully Integrated Dual-Output Continuously Scalable-Conversion-Ratio Switched-Capacitor Converter.**

Taehyeong Park and Chulwoo Kim

Korea University, Korea

CDC-P006 **A 97fsrms-Jitter, 8.16GHz Ring-Oscillator Injection-Locked Clock Multiplier with Power-Gating Injection-Locking**

Suneui Park, Yuhwan Shin, Jeonghyun Lee, and Jaehyouk Choi

Korea Advanced Institute of Science and Technology (KAIST), Korea

CHIP DESIGN CONTEST

CDC-P007 **A Heterogeneous Systolic-Vector Architecture with Resource Scheduling for Various DNN Workloads**

Jung-Hoon Kim, Sungyeob Yoo, Seungjae Moon, and Joo-Young Kim

Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P008 **An Ultra-Low-Power BiopotentialRecording Analog Front-End IC for Closed-Loop Neural Interfaces**

Donghoon Choi, Soonseong Hong, Hyojun Yoo and Hyouk-Kyu Cha

Seoul National University of Science and Technology, Korea

CDC-P009 **A 28nm Inverted Index Search Accelerator Chip with Applications to High-Performance Full-Text Search**

Sungjun Jung, Heo Jun, and Jae W. Lee

Seoul National University, Korea

CDC-P010 **A 13.56 MHz Wireless Power Transfer System with a Wide Operating Distance and Load Range for Biometric Smartcards**

Hongkyun Kim, Yechan Park, and Chul Kim

Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P011 **24-40GHz Gain-Boosted Wideband CMOS Down-Conversion Mixer Employing Body-Effect Control for 5G NR Applications**

Beomsoo Bae, Eunsoo Kim, Segyeong Kim, and Junghwan Han

Chungnam National University, Korea

CDC-P012 **A 900MHz Reconfigurable RF-DC Converter with Controllable Input Capacitor for RF Energy Harvesting**

Jongmin Park, Yosep Cho, and Jinwook Burm

Sogang University, Korea

CDC-P013 **A Single-TL, Bi-Directional, Simultaneous, Self skew-compensated and Multi-access Transceiver Architecture for Sensor Interface**

Seong-Min Ko and Dong-Woo Jee

Ajou University, Korea

CHIP DESIGN CONTEST

CDC-P014 **Scalable Deep-Learning Inference Processor based on Network-on-Chip**

Suchang Kim, Jaeyoung Lee, Hyejung Jang, Boseon Jang, and In-Cheol Park

Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P015 **The Design of a Programmable Embedded AI Processor with Cortex-M0**

Kwonneung Cho, Young Woo Jeong, Hyun Woo Oh, Chang Yeop Han, and Seung Eun Lee

Seoul National University of Science and Technology, Korea

CDC-P016 **35 GbpsESD Protection Circuit in 28nm CMOS Process**

Jaehoon Jeong, Hyungeun Kim, and Jinho Jeong

SogangUniversity, Korea

CDC-P017 **A DC-DC Converter using Self-Tracking Zero Current Detector and Two-Step Digital PWM**

Heon Bin Jang, Kee Hoon Yang, Jae Bin Kim, Jong Wan Jo, and Kang Yoon Lee

Sungkyunkwan University, Korea

CDC-P018 **Design of DRAM Refresh Prediction System**

Jonghyun Cho, Jihye Han, and Young-Jae Min

Halla University, Korea

CDC-P019 **Frequency-reconfigurable Low Noise Amplifier for mm-wave 5G with Inter-node Gm-boosting**

Seungchan Lee, Yeonseung Kim, and Songcheol Hong

Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P020 **ASK RF Receiver for ETCs with Hybrid ASK Modulator**

Kee-Hoon Yang, Tae-seob Oh, Jae-bin Kim, Jong-wan Jo, and Kang-yoon Lee

Sungkyunkwan University, Korea

CDC-P021 **A 5.8 GHz DSRC Wake-Up Receiver with an Intelligent Digital Controller**

Kee-Hoon Yang, Tae-seob Oh, Jae-bin Kim, Jong-wan Jo, and Kang-yoonLee

Sungkyunkwan University, Korea

CHIP DESIGN CONTEST

CDC-P022 **High Fill-Factor Dynamic Vision Sensor with Column-Parallel Readout**

Do-Won Kim and Byung-Geun Lee

GwangjuInstitute of Science and Technology(GIST), Korea

CDC-P023 **A 8-bit Loop Unrolled SAR ADC with Background Comparator Offset Calibration**

Seunghyun Kim, Yang Azevedo Tavares, and Minjae Lee

GwangjuInstitute of Science and Technology(GIST), Korea

CDC-P024 **Bit Parallel 6T SRAM In-memory Computing with Reconfigurable Bit-Precision**

Joonhyung Kim, Kyeongho Lee, and Jongsun Park

Korea University, Korea

CDC-P025 **A 9 V Output Three-Switch Hybrid Buck-Boost Converter using 5 V CMOS**

Hyunjin Kim, Taehyeong Park, and Chulwoo Kim

Korea University, Korea

CDC-P026 **mmWave Dual-Band Local Oscillator Buffer 5G New Radio Cellular Application**

Sengjun Jo and Kuduck Kwon

Kangwon National University, Korea

CDC-P027 **Face detection accelerator ASIC**

Jongkil Hyun,Kyeong-Kuk Min, and Byungin Moon

Kyungpook National University, Korea

CDC-P028 **Offset-Canceling Single-Ended Sensing Scheme for Resistive Non-Volatile Memory**

Bayartulga Ishdorj and Taehui Na

Incheon National University, Korea

CDC-P029 **An Adaptive Resolution Incremental ΔΣ ADC**

Jebeom Kim, Hyunkeun Lee, and Byung-Geun Lee

Gwangju Institute of Science and Technology(GIST), Korea

CHIP DESIGN CONTEST

CDC-P030 **A 140 GHz Low-Noise Amplifier based on 65 nm CMOS Technology**

Junghwan Yoo, Wooyong Keum, Heekang Son, and Jae-Sung Rieh

Korea University, Korea

CDC-P031 **Multi-Mode Radar RF Front-end Design**

Jinseop Lee, Ho Jin Kang, Chang Kyun Noh, Ha Jae Kwon, Yu Min Kim, Young Jin Kim, and Choon Sik Cho

Korea Aerospace University, Korea

CDC-P032 **Development of Ultra-Low Power 3D FPGAs for AI Computing**

Tae-Soo Kim, Yong-Bok Lee, and Jun-Bo Yoon

Korea Advanced Institute of Science and Technology(KAIST), Korea

CDC-P033 **A Design and Implementation of a Module-based CNN Accelerator**

Seong-Ho Jeon, Hyeok-Jun Kwon, and Seung-Ho Ok

Dong-EuiUniversity, Korea

CDC-P034 **A Power-and Area-Efficient DFE Receiver with Tap Coefficient-rotating Summer**

Won-Jong Choi, Geon-Hwi Lee, Un-Bok Wi, and Bai-Sun Kong

Sungkyunkwan University, Korea

CDC-P035 **Ultra-Low Power Delta-Sigma Modulator for Biomedical Applications**

Hwaseong Shin and Chiho Song, and Jeongjin Roh

Hanyang University, Korea

CDC-P036 **Design of High-Reliability LDO Regulator with Built-In Ultra Compact ESD Protection Circuit**

Sang Wook Kwon, Kyung-Il Do, and Yong-Seo Koo

Dankook University, Korea

CDC-P037 **600-GHz Pad-Embedded Imaging Array in 65-nm CMOS**

Doyoon Kim[1], Jai-Heon Cho[2], Kiryong Song[2], and Jae-Sung Rieh[1]

[1]*Korea University, Korea*
[2]*Samsung Electronics, Korea*

CHIP DESIGN CONTEST

CDC-P038 **A Psuedo-Differential High-Speed Sensing Scheme for Phase-Change Memory**

Myeong-Su Shin, Min-Seok Seol, and Bai-Sun Kong

Sungkyunkwan University, Korea

CDC-P039 **Watermark-Adaptive Image Watermarking Module based on Deep Learning**

Jae Eun Lee and Dong Wook Kim

Kwang Woon University, Korea

CDC-P040 **A 10-bit 2.5MS/s Pipelined ADC using 1.5-bit Multiplying-DAC in 0.18um CMOS Process**

Ji-Woo Park, Byeong-seok Kang, Sung Min Jang, and Young-Sik Kim

Handong Global University, Korea

CDC-P041 **A Ka-Band T/Rx Switch in 28-nm CMOS**

Youngjoo Lee and Byung-Wook Min

Yonsei University, Korea

CDC-P042 **A Ka-Band Variable Gain Amplifier in 28-nm CMOS**

Do Hoon Chun and Byung-Wook Min

Yonsei University, Korea

CDC-P043 **16 x 10 Pressure Sensor CMOS Driver IC to Minimize Resistance Interference of Adjacent Cells**

Jiseong Lee, Seoungsoo Kwak, Yun Chan Im, and Yong Sin Kim

Korea University, Korea

CDC-P044 **Two-negative feedback loop PLL with second-order filter**

Kyung-Seok Park and Young-Shig Choi

Pukyong National University, Korea

CDC-P045 **CMOS RF Energy Harvesting Rectifier Circuit using Body Bias Negative Feedback**

Daehan Lee and Yongchae Jeong

Jeonbuk National University, Korea

CHIP DESIGN CONTEST

CDC-P046 **24-40GHz mmWave Local Oscillator Buffer for 5G New Radio Cellular Application**

Hyunjun Kim and Kuduck Kwon

Kangwon National University, Korea

CDC-P047 **Coprocessor For AR/VR Equipment With Pose Estimation Function Using Kalman Filter**

Sun-Woo Jung, Yong-Bin Kim, and Seong-Soo Lee

Soongsil University, Korea

CDC-P048 **60-GHz Dual Polarization Capable OOK Receiver**

Geon Ho Park[1], Chul Woo Byeon[2], and Chul Soon Park[1]

[1]Korea Advanced Institute of Science and Technology (KAIST), Korea
[2]Wonkwang University, Korea

CDC-P049 **Pseudo-Static Gain Cell of Embedded DRAM for Processing-In-Memory**

Subin Kim, Jonghang Choi, Ingu Jeong, Yongjun Lee, and Jun-Eun Park

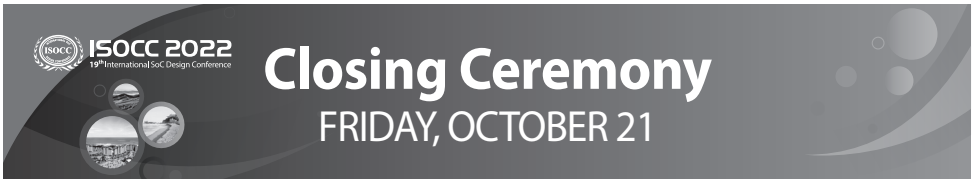
Chungnam National University, Korea

CDC-P050 **Vehicles with built-in IDS to compensate for CAN security vulnerabilities in CAN ECU**

Dae-gi Lee, Chang-Seon Han, and Seong-Soo Lee

Soongsil University, Korea

CLOSING CEREMONY



17:15~17:45 FRIDAY, OCTOBER 21, 2022
Lakai Ballroom 1 (Convention 1F)

Best Paper Awards

Best Poster Awards

Gift Drawing

10:00~11:00 SATURDAY, OCTOBER 22, 2022

SPECIAL PROGRAMS

Banquet

- **Banquet** at Skybay Hotel Gyeongpo will be provided to **all the on-site registrants** after the afternoon sessions on **Oct. 20,** respectively.

Date	Thursday, Oct. 20, 2022
Time	18:30-20:30
Venue	Skybay Hotel Gyeongpo, Grand Ballroom (L floor)

- The venue for the banquet is **"Skybay Hotel Gyeongpo"**. It takes about 5-10 minutes on foot from the main conference venue, Lakai Sandpine Resort.
- Please make sure that you have to show the **Banquet coupon in your name badge.** Conference attendee will get a banquet coupon together with the conference admission badge. Please be noted that you have to keep the coupon well and show it to the staff when having Banquet.
- All the conference registration includes an admission ticket for banquet.
- Extra ticket can be purchased at the registration desk. Ticket availability will depend on the available banquet spaces.

Additional Banquet Ticket	KRW 130,000/person (USD 100)

Banquet Performance

JAZZ BAND "PANDORA"

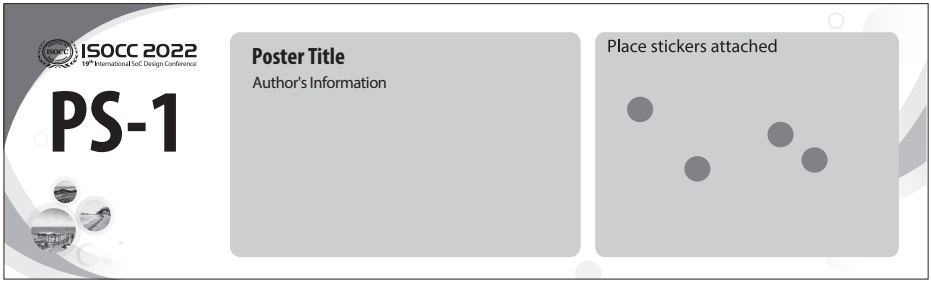
SPECIAL PROGRAMS

Most Popular Poster Voting

- **All on-site registrants can vote** by putting a small red sticker on the **"Place Stickers Attached" above each ISOCC Poster. More than one sticker can be added to any posters.**
- Inside your name tag, you will **find five red stickers** that can be used for this voting.
- Valuable gifts will be awarded at **the Closing Ceremony to the top-5 popular ISOCC Posters**

Date	Friday, Oct. 21, 2022
Time	17:15-17:45
Venue	Lakai Ballroom 1 (Convention 1F)

(Sample Image)



SPECIAL PROGRAMS

Gift Drawing

- **Gift Drawing** for conference attendants will be held during the **Closing Ceremony.**

Closing Ceremony	
Date	Friday, Oct. 21, 2022
Time	17:15-17:45
Venue	Lakai Ballroom 1 (Convention 1F)

(Sample Image)

Gift Drawing ticket
Don't lose it!

Put on ticket in the box
at Registration desk.

SAMSUNG Galaxy Book
(Core™ i5 / SSD 256GB)

SAMSUNG Galaxy Watch5 Pro
(45mm, Bluetooth)

SAMSUNG Galaxy Buds 2

JBL Go 3: Portable Speaker with Bluetooth

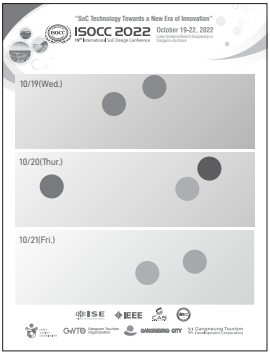
SPECIAL PROGRAMS

Gift for Session Participants

- A sticker for each attendee will be provided by our session staff at the end of each session including Tutorials, Short Tutorials, and Company Exhibition/Demo.
- We present **Starbucks Korea gift card** based on the number of stickers. Please do not miss this chance.
- You can receive the gift card at the registration desk.
- Please refer to the table below for the Starbucks Korea gift cards you can receive according to the number of stickers.

Date	Programs	The number of stickers by date.	Gift
Oct. 19 (Wed.)	- Mini/Main Tutorials - Afternoon Session	More than 2 Stickers	Starbucks Korea Gift Card of KRW 10,000
Oct. 20 (Thur.)	- Keynotes Speeches	More than 2 Stickers	Starbucks Korea Gift Card of KRW 10,000
	- CDC Oral Session - Afternoon Session-1 - Afternoon Session-2 - Afternoon Session-3 - Company Exhibition/Demo	More than 3 Stickers	Starbucks Korea Gift Card of KRW 10,000
Oct. 21 (Fri.)	- Morning Session	1 Sticker	Starbucks Korea Gift Card of KRW 10,000
	- Keynotes Speeches - Short Tutorial - Afternoon Session-1 - Afternoon Session-2 - Company Exhibition/Demo	More than 3 Stickers	Starbucks Korea Gift Card of KRW 10,000

(Sample Image)



Lunch

• Lunch at Lakai Sandpine Resort will be provided to all the **on-site registrants** after the morning sessions **on Oct. 20 and Oct. 21**, respectively.

Date	Thursday, Oct. 20, 2022	Friday, Oct. 21, 2022
Time	12:15-13:30	12:30-14:00
Venue	Hansong Hall (Reception B1F)	

• Please make sure that you have to show the **lunch coupon in your name badge.** Conference attendee will get a lunch coupon together with the conference admission badge. Please be noted that you have to keep the coupon well and show it to the staff when having lunch.

• Lunch locations may change. Please refer to the on-site guide.

Coffee Break

• **Coffee** will be served at the following hours.

Date	Thursday, Oct. 20 , 2022		Friday, Oct. 21, 2022	
Time	09:20-09:30	14:15-14:30	10:50-11:00	15:15-15:30
Venue	Convention 1F Lobby			

Download ISOCC 2022 Proceedings

• Download from ISOCC 2022 Website.

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2) Go to "Program" on ISOCC2022 Website, then go to "Program at a Glance" to download the proceeding ART Download" (**zip file)

• If you want to download the file to your USB or external drive, please ask our staffs at the registration desk.

• Please use your PC/MAC/Laptops for full access. (Not Accessible through smartphones)

CONFERENCE INFORMATION

Emergency Calls

Management Chair	Prof. Won-Yong Lee (Mobile: 010-3664-8514) Prof. Youngjoo Lee (Mobile: 010-6767-5718)
Police Services	112
Fire, Rescue & Hospital Services	119
First Aid Services	129
Medical Emergency	1339
Korea Travel Phone	1330

- **Our Staff** will be wearing the **uniform(Yellow Vest)** shown as below.

CONFERENCE VENUE MAP

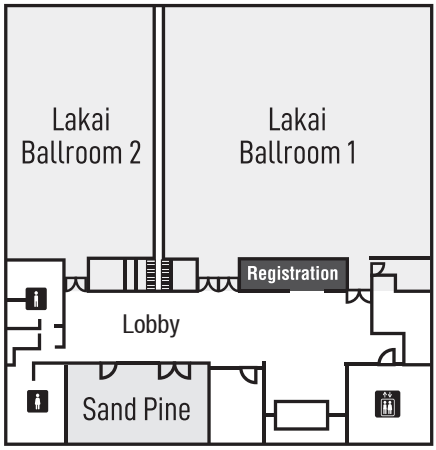
Venue

LaKai SANDPINE

- 536, Haean-ro, Gangneung-si, Gangwon-do, Korea
- Website: http://www.lakaisandpine.com/
- E-mail: lakaisandpine@sig.co.kr
- Tel: +82-1644-3001

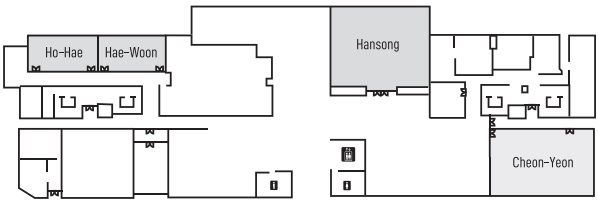
CONFERENCE VENUE MAP

1F Convention Hall



Lobby	Registration, Chip Design Contest(CDC), and Company Exhibitions
Lakai Ballroom 1	Opening & Closing Ceremony, Keynote Speeches, WiSoC
Lakai Ballroom 2	CDC Poster, ISOCC Poster
Sand Pine Hall	CDC ORAL, DCAS1~5, ML3
Ho-Hae Hall	SS1, SS3, SS5, SoC1, ET1, SS9, SS11, SoC2, ET2
Hae-Woon Hall	SS2, SS4, SS6, SS8, SS10, SS12, SS13
Cheon-Yeon Hall	Mini Tutorial, Main Tutorial, AC, DC, ML1, ML2, RF, WLN
Lunch	Hansong Hall(October 20~21)
Banquet	Skybay Hotel Gyeongpo, Grand Ballroom (1F)

B1 Tower5 Hall / Reception Hall

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The Institute of Semiconductor Engineers


IDEC
IC DESIGN EDUCATION CENTER


IEEE


CAS
IEEE CIRCUITS AND SYSTEMS SOCIETY

IEEE CASS Daegu Chapter

IEEE CASS Seoul Chapter

IEEE SSCS Seoul Chapter

KOREA
TOURISM
ORGANIZATION

GWTO Gangwon Tourism Organization

GANGNEUNG CITY

Gangneung Tourism
Development Corporation

자동차 · 조선 스마트 전자(ICT) 융합기술 교육연구단

충청북도 CHUNGCHEONGBUK-DO

cbist 충북과학기술혁신원
Chungbuk Innovation Institute of Science & Technology

청주대학교 CHEONGJU UNIVERSITY

청주대학교 SW융합클러스터사업단

4차산업혁명 선도를 위한 차세대 지능형 반도체 SW융합 플랫폼 조성

AI 반도체 프로세싱 SW 연구센터

AI Semiconductor Processing SW Research Center


AiPIM

KAIST 인공지능반도체시스템 연구센터
AI Semiconductor Systems Research Center

"미래 인공지능 사회를 위한 인공지능 반도체 핵심 원천기술및 응용 기술을 개발하고 석·박사급 전문 인재를 양성하는 것을 목표로 세계 최고 수준의 연구진, 국가의 전폭적 지지, 국내외 우수기관과의 협력, 다양한 창업 지원 등을 통하여, 미래 인공지능 사회를 위한 반도체기술을 세계적으로 선도하겠습니다."

인공지능반도체시스템 연구센터장 김 주 영

INHA UNIVERSITY

인공지능 시스템반도체 연구센터

DAEGU TECHNOPARK

MIIDS Research Center

AJOU Univ. 아주대학교

Medical Image-Based Intelligent Diagnosis Solution

인구 고령화로 인해 급증하는 의료비 지출을
지능형 의료 영상 솔루션 개발을 통해
의료비 절감에 기여합니다.

서울대학교 SEOUL NATIONAL UNIVERSITY

자동차향 시스템반도체 융합 인력육성 센터

Automotive System IC Fusion Human Resource Research Center

산학 밀착형 IoT 반도체 시스템 융합 인력육성 센터

● ISRC(IoT Semiconductor Research Center)의 소개

- ISRC컨소시엄 구성 : 총 **38개**(5개 대학교, 25개 산업체, 8개 기관)
- **최근 5년간 컨소시엄 기업 취직 : 참여 대학의 배출 인력 중 92%**
  (박사 87명, 석사 337명, 총 424명 중 391명)
- **지속적인 인력 공급 및 R&D 협력**으로 장기적인 상호 발전 가능

● 인력 육성의 목표 및 내용

센터의 인재상

폭넓은 교양은 물론
특정 분야 전문적인 자질을 갖춘

Generalist + Specialist

T자형 Intelligent BEST인재

Beyond **미래가치 창조**	기존의 가치를 뛰어넘는 **창의적 인재 육성**
Entrepreneurship **산업 밀착**	기업과의 프로젝트, PBL 통한 **밀착형 산학 연구**
Sharing **융합 및 교류**	융합 교육, 대학 간 학점 교류를 통한 **연구 리더 양성**
Top Class **세계 최고 수준**	글로벌 네트워크 교육 환경에 기반한 **최고 수준의 인재 양성**

센터의 목표

미래가치를 선도하는 First Mover로서
세계 최고수준의 IoT 반도체 연구를 Leading 할 수 있는
T자형 시스템 반도체 융합 전문인력육성을 목표

6년간 석사 130명, 박사 50명 양성
융합 교과목 60건 개설 및 신규 교재개발 108부

과학기술정보통신부 Ministry of Science and ICT

ISRC 산학 밀착형 IoT 반도체 시스템 융합 인력육성 센터
Corporate Intimated IoT Semiconductor System Fusion Human Resource Research Center

성균관대학교 컨소시엄

NRF 한국연구재단

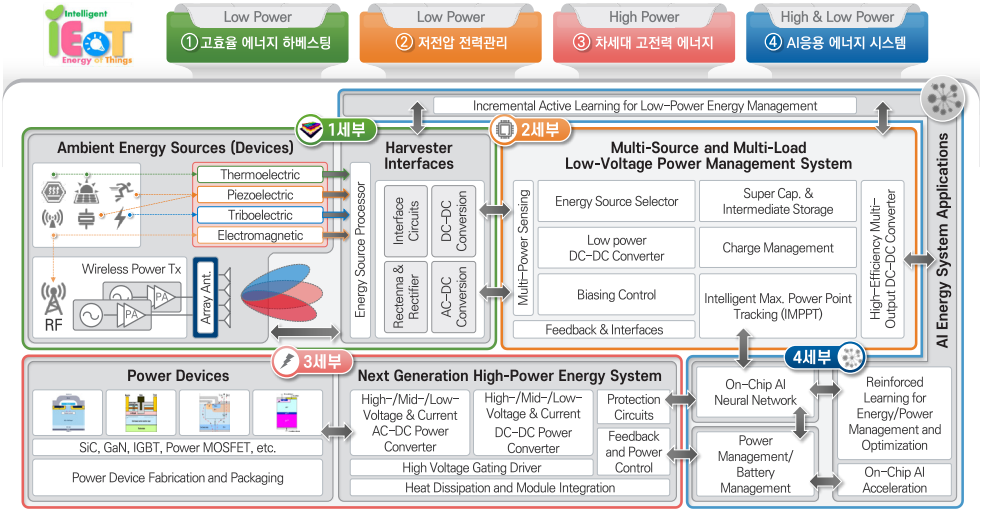
인공지능·반도체 시스템반도체 융합전문인력 양성센터


Value Creating University
POSTECH
Center for Biomedical System Semiconductor

지능형 사물 에너지 (iEoT) 시스템반도체 융합 다빈치형 인력육성 센터

Intelligent Energy-of-Things (iEoT) System IC Center for Da Vinci-type Convergence Education

에너지 시스템반도체 핵심 기술을 4개의 세부로 나누어 인력양성 추진



학제간 융합 및 PBL을 통한 'T자형' 인재 양성

지능형 에너지 반도체의 핵심 기술 분야를 4개 세부 주제로 나누고 6개 학과간의 학제간 융합 교육 및 PBL을 통한 심화연구를 바탕으로 T-자형 융합 전문인력양성

1세부 고효율 에너지 하베스팅

- 압전·마찰전기 에너지 하베스팅
- 광전·열전 에너지 하베스팅
- RF 에너지 하베스팅

2세부 저전압 전력관리

- 다중 에너지원 출력 관리 시스템
- 다중 에너지원 기반 MPPT 알고리즘 회로
- 스위치-커패시터 DC-DC 변환기

PBL

- Training MPW
- Practical MPW
- Chip Design Review (Seminar)

3세부 차세대 고전력 에너지 시스템

- 고전압 파워소자
- 고전력 에너지 시스템 구동 IC
- 고신뢰성 ESD 보호회로

4세부 에너지 시스템 AI기반 응용

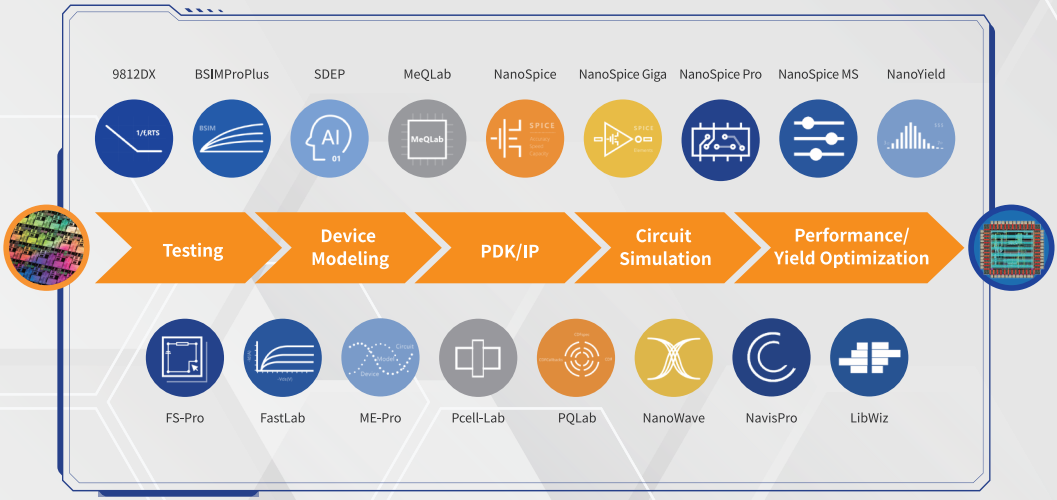
- 인공신경망 회로
- 능동적 학습 기반 저전력 에너지 관리
- 강화학습 기반 전력 최적화

과학기술정보통신부 중앙대학교 단국대학교 서강대학교 SOGANG UNIVERSITY 서울시립대학교 숭실대학교 UNIST 한국연구재단

대구대학교
DAEGU UNIVERSITY

PRIMARIUS

Leading Provider in Manufacture and Memory EDA



Innovative EDA Solutions to Bridge IC Design & Fabrication

www.primarius-tech.com


Infineon

High Speed Serial Test Solutions

LabMaster 10Zi-A 65GHz Oscilloscope

Protocol System

Automated transmitter testing for 56 Gb/s PAM4

PCIe 6.0 64 GT/s base Tx testing & Rx calibration

LPDDR2/3/4/5 physical layer testing

SDAIII-CompleteLinQ Analysis

Protocol Layer Debug &Test Solution for:

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DisplayPort , HDMI , Bluetooth & WIFI

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SKAi
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기술과 혁신을 통해 더 좋은 세상을 만들어 갑니다.


Power Solution
전원관리 최적솔루션 개발
Wireless Power, Energy Harvesting
솔루션 기반 기술


AI Solution
Neuromorphic 기반 AI 솔루션 개발
Analog PIM (Processor In Memory)
저전력, 소형기기 최적 AI 솔루션 개발


RF Solution
저전력, 저비용, 고성능 IoT 최적솔루션 개발
from BLE to 5G

배터리 교체가 필요없는 자동 무선 충전 솔루션

※ 제품군 : 에너지 하베스팅 전력관리반도체 PMIC(Power Management Integrated Circuit), 초저전력 마이크로 컨트롤러(MCU) (BY e-PEAS(벨기에))

산업

- 자산 추적기
- 스마트 물류
- 화재, 가스, 오염 센서
- 충돌방지 센서
- 전류 센서
- 탱크 모니터링 센서

사회농업

- 주차 센서
- 스마트 워치
- 무선 이어폰
- 온실 센서
- 동물 추적기 센서
- 가축 먹이 센서

홈오토메이션

- 자체 충전 리모컨
- 화재 경보
- 스마트 잠금 장치
- 모션센서
- 가스누출 모니터
- 스마트 주방장치

LoRa 표준 / 비표준 (Mesh)

표준

비표준

- LoRaWAN 표준 모듈 및 Gateway(network Server 포함)
- Mesh 방식의 LoRa 비표준 모듈 및 Gateway (모듈 간 통신 가능)
- LoRa 통신모듈, Gateway, Network Server 통합 솔루션 제공

SPD (Surge Protective Device)

- 모듈 교체식의 베이스 일체형 모듈타입
- 모듈에서 전원 차단시 탐지기능과 자동복구 기능의 자동복구형 누전 차단기
- 통신사 전력회사 등 다양한 산업군에 적용 가능

SIT TECHNOLOGY INC.
(주)에스아이티 테크놀로지 경기도 안양시 동안구 경수대로 574(호계동, 윤성빌딩 6층)
TEL : 031-425-2780 | HP : 010-5501-7896 | E-mail : apollo2@sittech.co.kr

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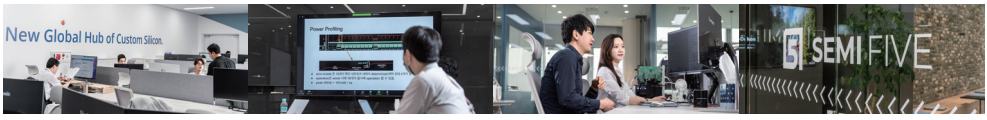
Founded in Seoul in 2018, SemiFive is basing its foundation on Korea's semiconductor design competency that was amassed for more than 20 years. With expertise in front-end to back-end design, SemiFive has become the fastest growing silicon design company that offers the most comprehensive services. SemiFive's core business is its innovative Platform SoC that enables low-cost & high-efficiency SoC design, and also provides various design solutions for global customers through its diverse network. As the cost of developing an SoC and the demand for customized silicon continue to grow rapidly, SemiFive's Platform SoC will play a key role in turning innovative ideas into silicon.

SemiFive, hand in hand with global innovation leaders, strives to become a leading partner for future SoC designs, and thereby becoming: the New Global Hub of Custom Silicon



SEMIFIVE, Korea
info@semifive.com

SEMIFIVE, US
us@semifive.com

Address 2F, Korea Design Center, 322 Yanghyunro, Bundang-gu, Seongnam-si, Gyeonggi-do, Republic of Korea, 13496

Website

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rebellions_

AI Development System

PRESTO-AI Server

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FPGA Based Deep Learning Inference Solution

Zebra

- Faster AI Inference Computation than GPUs
- Consistent Performance & Lower Cost
- Plug & Play ML Inference Aceleration
- Zero FPGA Knowledge

Mipsology

All-in-One System

Host System
Intel / AMD Processor

H/W Accelerator Card
ALVEO / GPU Card

Pre-installed Software Pack
OS, Design Tool, Framework, Driver, Library, etc.

이기종 AI 가속기

Accelerator Card
NVIDIA / AMD GPU Card
ALVEO Card for Inference

공식 교육 기관

AMD-Xilinx Training Center
AMD-Xilinx 공식 교육 제공
AMD-Xilinx Partner 솔루션 및 기술 지원

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ML / HPC
1,728K LUTs
12,288 DSP Slices
64GB DDR

ALVEO U55C
ML / HPC
1,304K LUTs
9,024 DSP Slices
16GB HBM

Smart SSD
Computational Storage
300K LUTs
1,968 DSP Slices
3.84 TB

ALVEO U50
ML / HPC / FinTech
872K LUTs
5,952 DSP Slices
8GB HBM

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DEVELOPMENT TOOLS AND SOFTWARE

arm KEIL

ARM은 영국 기업으로, ARM 아키텍처를 설계하고 라이센스를 판매하며 시스템 플랫폼과 SoC의 HW/SW를 개발하는 반도체 기업입니다.

ARM DEVELOPMENT STUDIO

One Tool Suite,
Any Arm Project

	Bronze	Silver	Gold
Arm Processor Support			
Cortex-A/R Armv8		○	○ ●
Cortex-A Armv8 (selected cores*)	○	○	○ ●
Cortex-A/R Armv7	○	○ ●	○ ●
Cortex-M Armv6/7/8	○ ●	○ ●	○ ●
Previous Arm architectures*	○ ●	○ ●	○ ●
KEIL MDK	Essential edition	Professional edition	Professional edition
Middleware		✔	✔
CMSIS-RTOS RTX with full source code	✔		✔

KEIL MDK

Accelerated MCU
Software Development

Edition	MDK Professional	MDK Plus	MDK Essential
Ideal for	Fastest route to market and/or functional safety applications	Development on mainstream Arm MCUs	Entry-level professional development on Cortex-M
Target devices	All Arm Cortex-M, Armv8-M, SecurCore and legacy Arm MCUs – including Fast Models	All Arm Cortex-M, SecurCore and legacy Arm MCUs	All Arm Cortex-M, non-secure
Host platforms	Windows	Windows	Windows
Middleware	Full Featured	Basic	

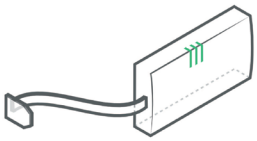
DSTREAM

High Performance
Debug and Trace

Features and Benefits

- Broad Arm Architecture Support
- Built for Arm Tools
- High-bandwidth CoreSight trace

ULINK FAMILIES DEBUG AND TRACE UNIT

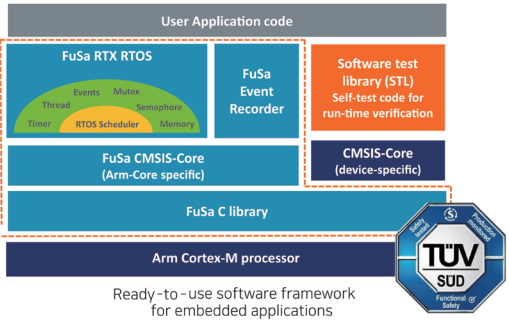


Versatile Microcontroller Debug

Features and Benefits

- Broad Device Support
- Robust Debug Capabilities
- Fast Connections

RTX



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for embedded applications

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Faster time-to-market

Optimized by the architecture experts

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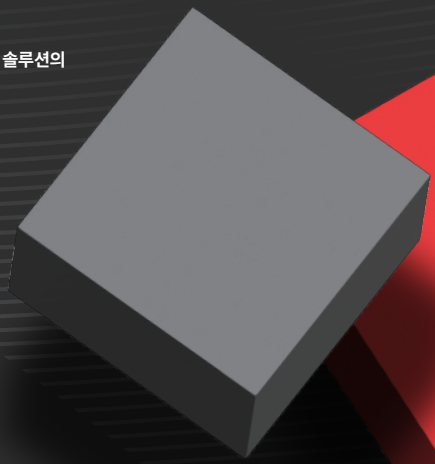
실리콘마이터스는 고성능/고효율 스마트 PMIC(전력관리 통합 칩) 솔루션의
상품기획 및 개발, 제조를 전문으로 하는 팹리스 회사로서 이를 통해
스마트폰 및 Tablet, TV, 노트북, 모니터, Automotive, IoT 등
다양한 전자제품에 최적의 전력관리 솔루션을 제공합니다.



실리콘마이터스와 함께
꿈과 미래를 같이 할 인재를 초빙합니다.

모집분야	자격요건
Power / Analog 및 Mixed Signal 반도체 집적회로 설계	신입 (석사, 박사 및 졸업예정자)
Digital Logic 반도체 집적회로 설계	경력 (학사이상)

문의 및 접수는 실리콘마이터스 인사팀(070-7844-3500,hr@siliconmitus.com)에서
친절히 도와드리겠습니다.

*병역특례(전문연구요원) 지원가능

경기도 성남시 분당구 대왕판교로 660 유스페이스 1 A동 8층 I 대표전화 1670-7665 I www.siliconmitus.com


센서위드유
SENSOR WITH U

SAPEON

대한민국 최초 데이터센터용 AI 반도체

SERVER

SAPEON X220

AI Inference

2021

SERVER

AI Training/Inference

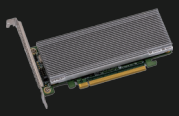
IP

AI Inference

EDGE

AI Inference

2023



X220 Compact Card

X220 Enterprise Card

Chip, Card, Server, Cloud 형태로 제공

Specification

Int8 Performance	87 Tera OPS Boost Mode 106 Tera OPS
Precision	INT 16/8/4
Effective Performance (Resnet-50)	6.7K FPS
Memory Capacity	8 GB
Host Interface	PCIe Gen3 16 Lane
Max Power Consumption	65 W

MLPerf v2.1 Benchmark Results

Datacenter Inference Server (Resnet-50)

Use case

DATACENTER	**데이터센터 내 AI 클라우드 서비스** 기존 시스템 대비 처리속도 1.3배 증가
MEDIA	**영상 화질 개선 (AI Upscale)** 기존 시스템 대비 인프라 비용 42% 절감
SECURITY	**객체 탐지 알고리즘** 기존 시스템 대비 2.3배 성능 개선
MOBILITY	**VLAM (영상기반 위치 측위 솔루션)** 실시간 추론 성능 극대화
FACTORY	**스마트 팩토리** AI 기반 불량 탐지 시스템
ROBOT	**물류 배송 로봇** **자율 주행 로봇**

* Normalized to 경쟁사 가속기 (진핵소모 및 규격면 유사 스펙의 최신 제품)

Source: https://www.sapeon.com/post/sapeon-newsroom-mlperf MLPerf™ Inference v2.1 Results | MLPerf ID 2.1-0109, 2.1-0110, 2.1-0011

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Nextchip is the automotive fabless company
mainly developing technologies for camera sensor from human vision to computer vision.
Nextchip can guarantee and provide you the most optimized vision based ADAS processors.

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네오와인은 보안반도체 설계 및 공급사로 복제방지반도체, IoT 보안 반도체 및 MCU를 시장에 공급, 누적으로 1.2억개의 보안 반도체를 2000개 이상의 기업고객에 공급하고 있는 펨리스 회사입니다.

PRODUCT

Anti-replication IC Protection of system software from illegal replication

AEC-Q100인증

ALPU-CV IC for electrical components of cars

- High performance illegal anti-replication IC
- Unique Group ID/Serial No., I2C, SOT23-6L, Power (1.8/3.3V)

ALPU-C IC to prevent illegal copy of system S/W of electronic devices

- High performance illegal anti-replication IC
- AES-128 , 128bit OTP cells
- Active/Sleep mode, I2C, Power (1.8/3.3V), SOT23-6L

GEN-FA Anti-replication IC with memory

- User programmable anti-replication IC
- AES-128, SHA-256, 32Kbits EEPROM, I2C, Power 3.3V

ALPU-A1M Raspberry Pi based Anti-replication Module

- Active/Sleep mode, I2C, Power (1.8/3.3V), SOT23-6L
- User programmable anti-replication IC
- AES-128, SHA-256, 32Kbits EEPROM, I2C, Power 3.3V

IoT Security IC IoT device data protection

KCMVP인증

DALPU-4 Public key based encryption semiconductor

- ECC, RSA, AES, SHA, TRNG, PUF, USB, SPI, 128KB EEPROM , 32KB SRAM
- Package: QFN 4x4-25L (4mm X 4mm X 0.75mm)

DALPU-D4M IoT security module for Raspberry Pi

- ECC, RSA, AES, SHA, 128KB EEPROM , 32KB SRAM

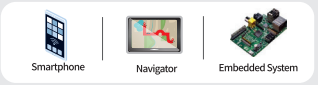
MCU Wireless charging, Embedded system

NWC01N56W48K wireless charging IC

- 32bit CPU, 48KB EEPROM, 6KB SRMA, 12C, GPIO
- Package : 56 QFN

NWT07N42G32K MCU for Embedded system

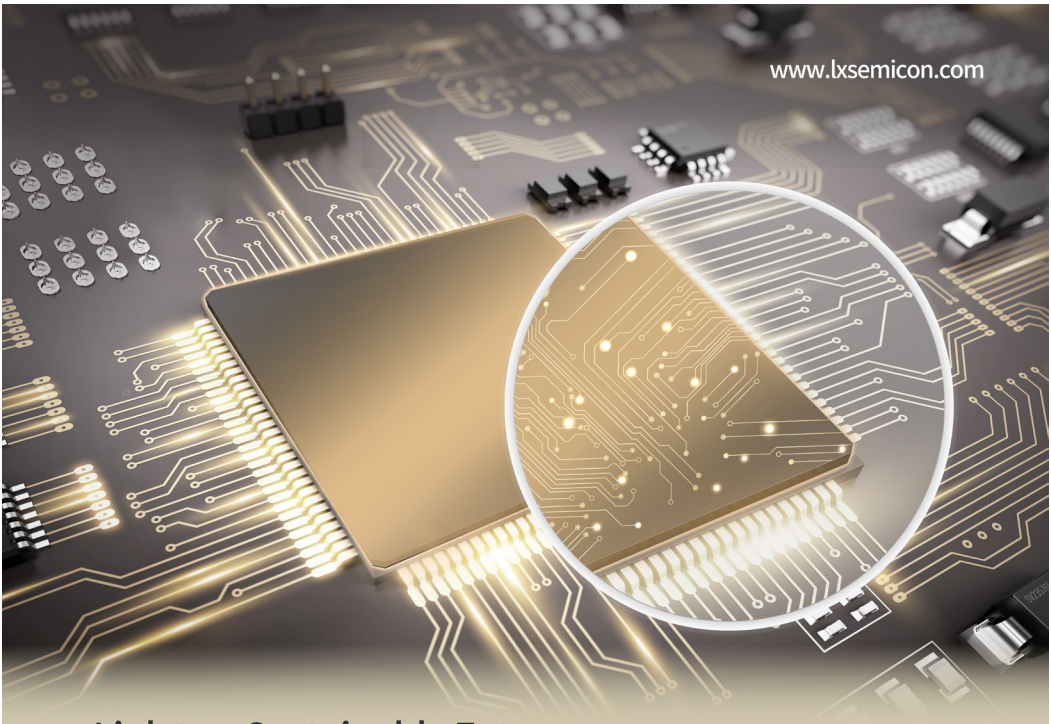
- ARM7TDMI, 32KB EEPROM, 4KB SRAM, DMA, I2C, SPI,GPIO
- Package : 4.5x4.5 uTQFN



NWT07N42T32K Capacitive Touch Screen Controller IC

- 32bit ARM CPU, 32KB ROM, 4KB SRMA, DMA, I2C, SPI, GPIO
- Package : 4.5x4.5 uTQFN, 26-Channel

주소 경기도 성남시 분당구 백현로 97 (수내동 22-3) 1206호 | **전화** 031-706-8484 | **팩스** 031-706-8485 | **사업문의** dexter@neowine.com | **www.neowine.com**



Link to a Sustainable Future

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LX세미콘이 시스템반도체로 열어가겠습니다.

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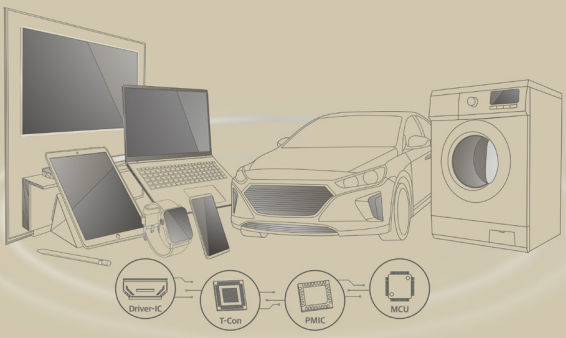
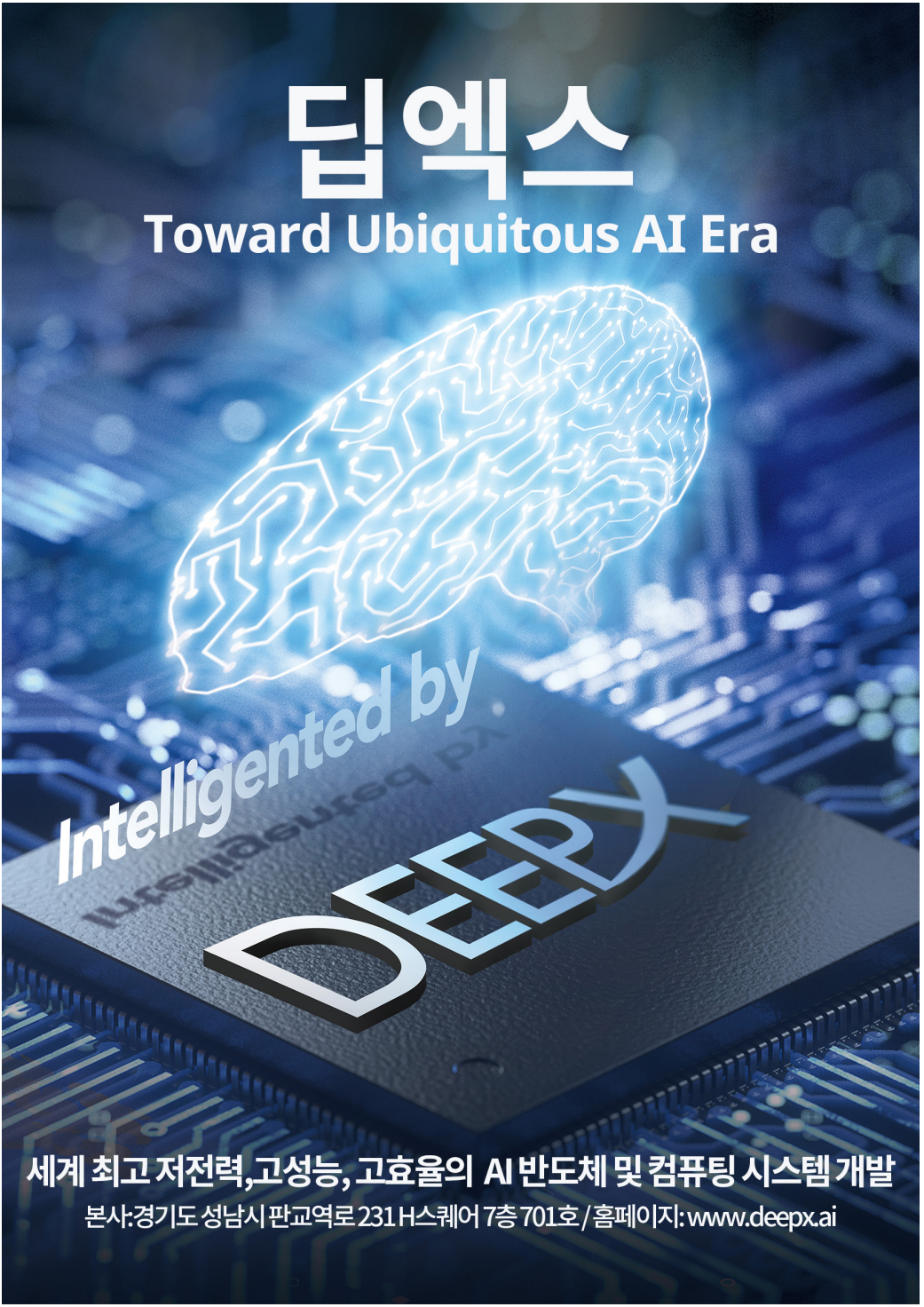
시스템반도체 기술로 국내 팹리스를 대표하는 기업으로 성장하고 있습니다.



LX세미콘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- Board Level Design
- BSP/SDK Design

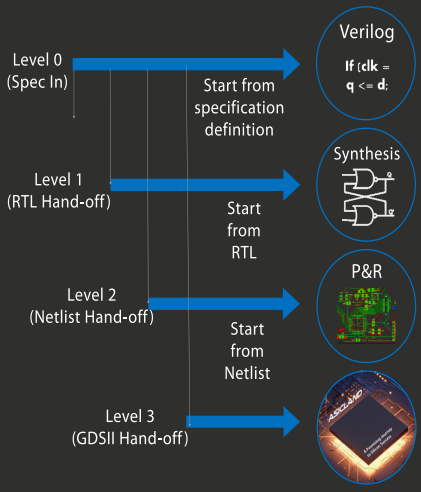
DS (Design Service)

Front-End
- Synthesis
- Static Timing Analysis
- Equivalence Check
- Design for Testability

Back-End
- Auto Place & Routing
- Timing Optimization

Design For Test
- SCAN
- ATPG
- Memory BIST / BIRA

Design Service Level



PM (Product Management)

Project Enabling & Technical Support
- Project schedule management
- Technical requirement & Tape-out supporting

IP Development
- IP Survey
- Develop Custom IP

PKG & QA Service
- Package Design
- Failure Analysis & Reliability Test

Test Service
- Wafer Test
- Final Test

Our Partner	IP Ecosystem	Package Service	Test Service	Reliability Service
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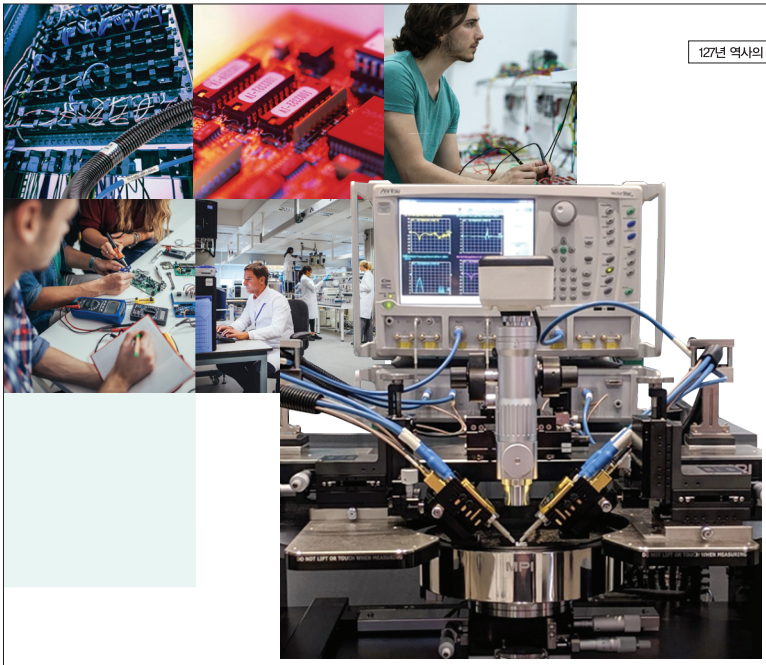
	Rambus	Signetics	GMTEST	
	cadence	ATsemicon	ADVANTEST	
	LG INCUBATION	HANA MICRON	TERADYNE	

127년 역사의 계측기 명가 안리쓰가 6G에도 함께 합니다



70 kHz to 220 GHz Broadband VNA Solution

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안리쓰의 RF광대역 시스템은 세계 최고 수준의 다이내믹 레인지, 정확도, 정밀도, 안정성을 제공합니다.

Key Applications

- 6G Device 모델링
- 광대역 Optical to Eletronic & Eletronic to Optical 테스트 (실리콘 포토닉스)
- 반도체 소자 모델링, On-wafer 테스트
- 고주파 소재 물성 테스트

* Sequential Simultaneous Display
(S-파라미터, TDR, Eye-daigram, Spectrum analyzer) 지원
* US CA(본사)에서 70 kHz to 220 GHz 4Port True-RMS
셋업을 통한 On-wafer 테스트 지원

220GHz까지 가장 넓은 주파수 범위, 1.1THz까지 확장

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모듈식 아키텍처를 통해 필요에 따라 시스템 확장 가능

장치 모델링에서 도파관 대역 외삽 오류의 위험 감소

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기업소개

어보브반도체는 “고객중심의 도전과 혁신 " 의 경영이념을 바탕으로 세계 MCU 시장의 정상의 자리에 도전하기 위하여 끊임없는 기술 개발과 R&D 투자로 고객과 함께 새로운 시장을 창출해 나가고 있는 MCU(Micro Controller Unit) 전문 반도체 기업입니다.

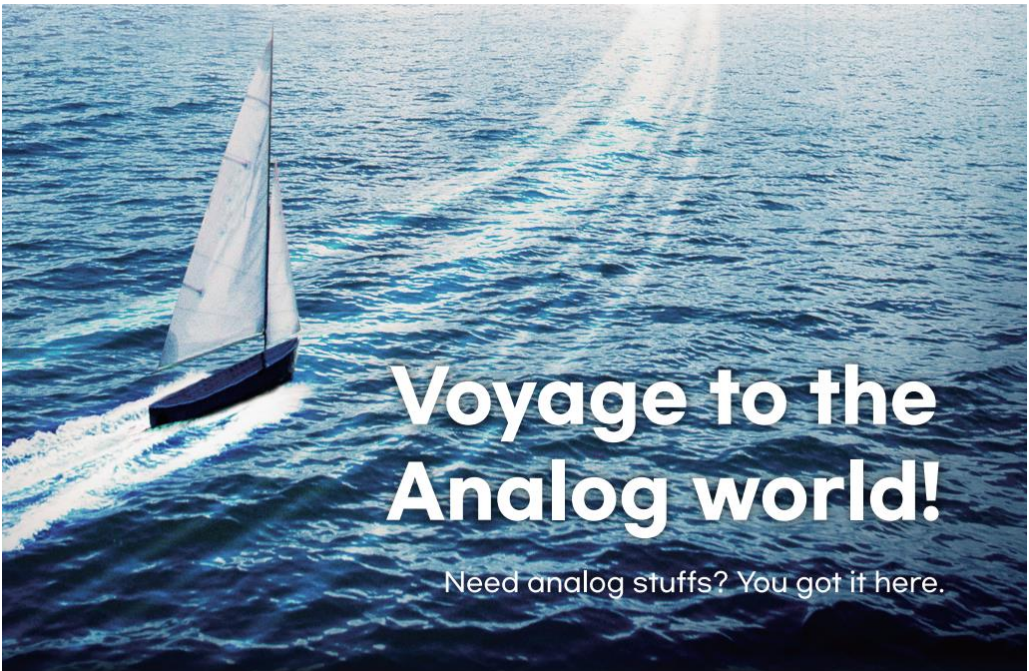
LG반도체 시절부터 30여 년을 함께 해 온 어보브반도체의 기술과 경험, 노하우는 국내외 IT 산업 발전의 디딤돌이 되었으며, 나아가 4차 산업혁명의 핵심 아이콘으로 새로운 디지털 세상을 견인하고 있습니다.

채용정보

모집분야	직무 내용	담당 업무
MCU 반도체 설계	[디지털 / 아날로그] 회로 설계	8비트 및 32-비트 MCU 설계 디지털설계 개발 도구 - RTL(Verilog) / FPGA / Synopsys / Cadence 아날로그설계 개발 도구 - Cadence / Hspice / Calibre
MCU 반도체 응용설계	반도체 응용설계(FAE / AE)	Analog 신호 처리, 반도체 응용 검증 개발 툴 개발 8Bit, 32Bit MCU 검증 및 개발 지원

- 근무지 : 서울 강남구 대치동 (2호선 삼성역)
- 산학연계 장학생 운영(산학연계 인력양성 프로그램)
- 병역특례 지정업체 : 전문연구요원
- 어보브반도체 홈페이지(www.abov.co.kr) 채용절차 참조(이메일 지원)


Telechips



테크위드유
신입 및 경력직원 채용 공고

Analog 설계

담당업무

- CMOS Analog circuit design (ADC, DAC, PLL, OSC, DCDC, LDO, LVDS, PWM 등등 상기 언급된 IP중 유경험자)
- HSPICE & Spectre 사용 가능자
- Layout설계 또는 설계 guide 가능한 자
- 회로 불량분석 및 양산 경험자

지원자격

- 경력 : 경력 1년 ~ 10년 (연구원, 선임연구원, 책임연구원급)
- 기타 필수 사항

우대사항

- 전기/전자공학, 컴퓨터/시스템공학
- 해당직무 근무경험
- 석사학위 수여자, 박사학위 수여자
- 유관업무 경력자
- 인근거주자
- 즉시출근 가능자
- 장기근무 가능자

Digital 설계

담당업무

- ASIC설계 유경험자, RTL coding, MCU제품개발, FPGA Handle, ASIC제품개발

지원자격

- 경력 : 경력 1년 ~ 10년 (연구원, 선임연구원, 책임연구원급)
- 기타 필수 사항

우대사항

- 전기/전자공학, 컴퓨터/시스템공학
- 해당직무 근무경험
- 석사학위 수여자, 박사학위 수여자
- 유관업무 경력자 · 인근거주자
- 즉시출근 가능자 · 장기근무 가능자

유경험자 우대

- TOP integration 경력자
- Sensor I/F: DSP (Digital filter, AFE control logic, external I/F, etc)
- MCU (ARM Cortex-M0/ M3을 embed한 mixed-IC 설계)
- 기타 mixed-signal IC용 control logic 설계

Application Engineer 설계

담당업무

- 반도체 IC 평가용 PCB 설계 및 검증
- MCU Control F/W 개발
- 계측 장비를 통한 반도체 검증 및 평가
- Final TEST Setup
- TEST Yield 관리 및 개선

지원자격

- 경력 : 경력 2년 ~ 5년(연구원, 선임연구원)
- 기타 필수 사항

우대사항

- 전기/전자공학, 컴퓨터/시스템공학
- PADs 및 OrCAD 경험자
- 반도체 양산 관리 경험자
- Labview 경험자
- 해당직무 근무경험
- 유관업무 경력자
- 즉시출근 가능자
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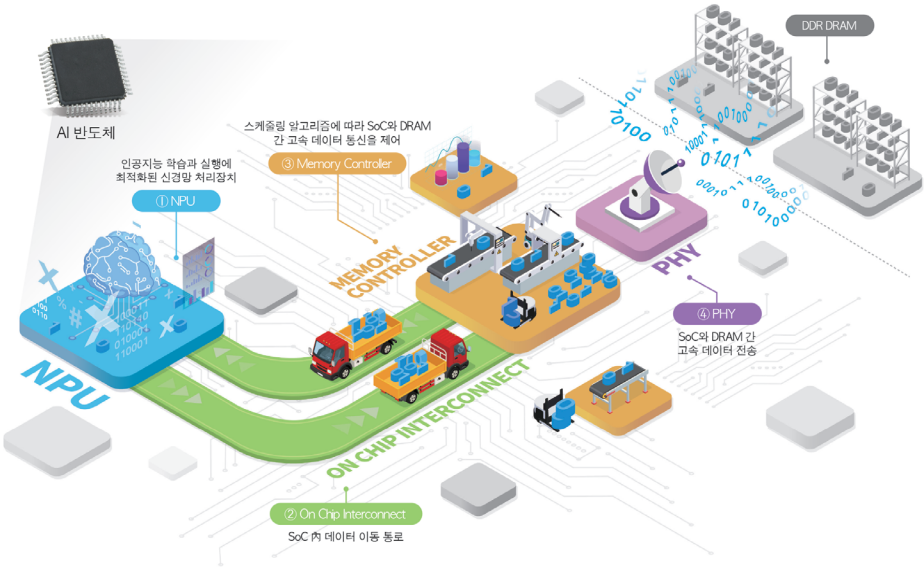
3. Memory Controller IP - 스케줄링 알고리즘에 따라 SoC와 DRAM 간 고속 데이터 통신을 제어
4. DDR PHY IP - SoC와 DRAM 간 고속 데이터 전송

반도체 분야 최초 기술평가 AA등급 취득

세계 유일 AI 반도체 통합 IP 솔루션 제공

검증된 글로벌 Track Record

글로벌 기업과의 전략적 파트너십



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